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ATTORNEY'S DOCKET NUMBER: 501.40474X00 filed August 16, 2001

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INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP99/00929	26 February 1999 (26.02.99)	

TITLE OF INVENTION: DIGITAL SIGNAL RECORDED, REPRODUCER AND RECORDING MEDIUM

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Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND or SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [X] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is attached hereto (required only if not communicated by the International Bureau).
   b. [X] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [X] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [ ] Amendments to the claims of the International Aplication under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [ ] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [ ] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16. [X] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [X] Other items or information:

See Attachment 1

U.S. APPLICATION NO (if known, see 37 CFR 1.5) 09/913595	INTERNATIONAL APPLICATION NO PCT/JP99/00929	ATTORNEY'S DOCKET NUMBER 501.40474X00

21. ☒ The following fees are submitted:	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a (2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1000.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(l)-(4) **$690.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 0.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	46 -20 =	26	x $18.00	$ 468.00	
Independent claims	8 -3 =	5	x $80.00	$ 400.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $270.00	$ 0.00	
TOTAL OF ABOVE CALCULATIONS =				$ 1,728.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.			+	$ 0.00	
SUBTOTAL =				$ 1,728.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				$ 0.00	
TOTAL NATIONAL FEE =				$ 1,728.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$ 0.00	
TOTAL FEES ENCLOSED =				$ 1,728.00	
				Amount to be refunded:	$
				charged:	$

a. ☐ A check in the amount of $ _____ to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 01-2135 . A duplicate copy of this sheet is enclosed.

d. ☒ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

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DIGITAL SIGNAL RECORDER, REPRODUCER AND RECORDING MEDIUM

BACKGROUND OF THE INVENTION

This invention relates to a digital signal recorder, reproducer, and recording medium, and more particularly to a recorder, reproducer, and recording medium having a function for protecting the copyrights of digital signals on a recording medium.

Research has been advanced in recent years on the compression of data such as video and audio which employ digital technology, and it has become easy to store and transmit these data. In conjunction therewith, digitization is also being rapidly advanced in the field of broadcasting.

Systems are known, for example, for very efficiently converting analog video signals to compressed digital code, using the MPEG (Moving Picture Experts Group) standard, and transmitting the compressed digital signals via satellite or coaxial cables. A digital broadcast receiver called a set top box is available as an apparatus for receiving these digital broadcasts.

In the field of video and audio signal recording and reproducing equipment, advances are being made in the development of digital VTRs that, using magnetic tape, can record and reproduce video and audio signals that have been converted to compressed digital code, such as digital TV broadcasts, in their digital signal form.

The digital broadcast receiver and digital VTR here are connected by a digital interface, making it possible to save received digital broadcasts without sacrificing their high quality.

Technology wherewith a transmitted digital signal in which a plurality of information is multiplexed is received and a desired program is selected therefrom is described in Japanese Patent Application Laid-Open No. H8-56350/1996. And a digital VTR that uses a rotary magnetic head is described, for example, in Japanese Patent Application Laid-Open No. H5-174496/1993.

Also, a digital broadcast recording system wherein a digital broadcast receiver and a digital VTR are connected by a digital interface is described in detail in "Newly Developed D-VHS Digital Tape Recording System for the Multimedia Era," *IEEE Transactions on Consumer Electronics*, Volume. 42, No. 3, August, 1996, pp 617-622.

Nevertheless, no consideration whatever has been given in such prior art to copyright protection for digital signals recorded on a recording medium by a digital VTR or the like from a digital broadcast or the like.

An object of the present invention is to protect the copyrights of digital signals on a recording medium.

SUMMARY OF THE INVENTION

The present invention, in a digital signal recorder for recording a digital signal on a recording medium, a digital reproducer for reproducing such signal, and a recording medium, at recording time, encrypts the digital signal with a key obtained by

subjecting key information to a prescribed arithmetic operation, and records the digital signal together with the key information on the recording medium, and, at reproducing time, decrypts the reproduced digital signal with a key obtained by subjecting the key information reproduced from the recording medium to the prescribed arithmetic operation.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram of a configuration comprising a digital broadcast receiver and a digital signal recorder-reproducer, in an embodiment of the present invention;

Fig. 2 is a diagram of configuration of a digital signal recorder and reproducer 200 of Fig. 1;

Fig. 3 is a diagram of a configuration of a compressed digital video signal packet;

Fig. 4 is a diagram of a configuration of the packet header 306 indicated in Fig. 3;

Fig. 5(a) and 5(b) are diagrams of configurations of a digital broadcast transmission signal and of a signal selected from a transmission signal;

Fig. 6 is a diagram of a configuration of the data encryption circuit 115 indicated in Fig. 2;

Fig. 7 is a diagram of a configuration of the encrypter 1155 indicated in Fig. 6;

Fig. 8(a) and 8(b) are diagrams of the generation of data keys in a control circuit 104 which represent cases of the

generation of data keys sent to the data encryption circuit 115 and the data decryption circuit 116 indicated in Fig. 2;

Fig. 9 is a diagram of a recording pattern on 1 track in a tape 111;

Fig. 10 is a diagram of a configuration of a block in the data recording area 7 indicated in Fig. 9;

Fig. 11 is a diagram of a configuration of the ID information 21 indicated in Fig. 10;

Fig. 12 is a diagram of a configuration of 1 track of data in the data recording area 7 indicated in Fig. 9;

Fig. 13 is a diagram of a configuration of blocks in 1 packet when a compressed digital video signal transmitted in a 188-byte packet format is recorded in the data 41 indicated in Fig. 12;

Fig. 14 is a diagram of a configuration of the header 44 for the data recording area 7 indicated in Fig. 12;

Fig. 15 is a diagram of a configuration of pack data when block keys are held in the auxiliary information 47 area indicated in Fig. 14;

Fig. 16 is a diagram of a method for holding block keys;

Fig. 17 is a diagram of another method for holding block keys;

Fig. 18 is a diagram of a specific configuration for the time information 25 indicated in Fig. 13;

Fig. 19 is a diagram of a configuration of the data decryption circuit 116 indicated in Fig. 2;

Fig. 20 is a diagram of a configuration of a digital recording and reproducing signal processing circuit 102 comprising the recording signal processing circuit 102a and the reproducing signal processing circuit 102b indicated in Fig. 2;

Fig. 21 is a timing chart for signal processing when data recording is started;

Fig. 22 is a diagram of key information in the tape 111 indicated in Fig. 2;

Fig. 23 is a timing chart for signal processing when reproducing data; and

Fig. 24 is a diagram of another configuration of the digital signal recorder-reproducer 200 indicated in Fig. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention is now described with reference to the drawings.

Fig. 1 is a diagram of a configuration comprising a digital broadcast receiver and a digital signal recorder-reproducer. Item 200 is the digital signal recorder-reproducer, 201 is a digital broadcast receiver, 202 is an antenna, and 207 is a video monitor. Item 203, moreover, is a tuner, 204 is a selector circuit, 205 is a decoder, 206 is an interface circuit, and 208 is a control circuit for controlling the operation of the digital broadcast receiver 201. The digital broadcast receiver 201 and the digital signal recorder-reproducer 200 here are represented as separate configurations, but these may be integrated into a single configuration.

Fig. 2 is a diagram of a configuration of the digital signal recorder-reproducer 200 indicated in Fig. 1. Fig. 2 diagrams an apparatus that is used for both recording and reproducing, but there will be no difference if recording and reproducing are made independent. Item 100 is a rotary head, 101 is a capstan, 102a is a recording signal processing circuit for performing such as the generation of recording signals when recording, 102b is a reproducing signal processing circuit for performing such as the demodulation of reproducing signals when reproducing, 104 is a control circuit such as a microprocessor, for example, for controlling recording and reproducing modes, etc., 105 is a timing generator circuit for generating a timing signal that becomes a reference for the turning of the rotary head 100, etc., 106 is a servo circuit for controlling the rotary head and the feed speed of tape, 107 is an input/output circuit for inputting recording signals and outputting reproducing signals, 109 is a timing control circuit for controlling timing when recording, 110 is an oscillator for generating a reference clock signal, 111 is a tape, 112 is an analog video signal recording and reproducing circuit, 115 is a data encryption circuit used when recording a digital signal, 116 is a data decryption circuit used when reproducing a digital signal, 117 is a device key generator for generating device keys that become a basis for data keys sent to a data encryption circuit 115 or data decryption circuit 116 when encrypting or decrypting digital information, 118 is a block key generator for generating block keys that become another basis for data keys when encrypting

or decrypting digital information, and 119 is an input/output control circuit for performing a time stamping routine when recording and performing packet data output control when reproducing.

Compressed digital video signals are transmitted as packet-formatted data wherein signals of multiple channels are time-division multiplexed. In Fig. 1, a digital broadcast signal received by the antenna 202 is demodulated by the tuner 203, after which a necessary compressed digital video signal is selected by the selector circuit 204. The selected compressed digital video signal is decoded by the decoder 205 to an ordinary video signal and output to the video monitor 207. When the received signal has been subjected to scrambling processing or the like, the signal is decoded after being descrambled in the selector circuit 204. When a received digital broadcast signal is recorded, the compressed digital video signal to be recorded and information pertaining thereto are selected in the selector circuit 204, routed through the interface circuit 206, input through an input/output terminal 108 of the digital signal recorder-reproducer 200 to the digital signal recorder-reproducer 200, and recorded. When reproducing the recorded digital broadcast signal, the compressed digital video signal reproduced by the digital signal recorder-reproducer 200 is output from the input/output terminal 108 to the interface circuit 206. The compressed digital video signal input to the interface circuit 206 is subjected to the same kind of processing as during

ordinary reception, by the selector circuit 204 and the decoder 205, and output to the video monitor 207.

In Fig. 2, which diagrams the configuration of the digital signal recorder-reproducer 200 indicated in Fig. 1, when recording, part of the packet data input from the input/output terminal 108 is input via the input/output circuit 107 to the control circuit 104. In the control circuit 104, the packet data type and such like are detected from information that is added to the packet data packet data or information sent separately from the packet data, a recording mode is determined according to the detection results, and the operating mode of the recording signal processing circuit 102a and servo circuit 106 is set. Next, the input/output circuit 107 outputs the packet data to be recorded to the data encryption circuit 115. In the data encryption circuit 115, the input packet data are encrypted, by a data key generated in the control circuit 104 based on keys generated by the device key generator 117 and the block key generator 118, and those encrypted data are output to the input/output control circuit 119. In the input/output control circuit 119, a time stamp is added in the packet data input, based on time information from the timing generator circuit 105, and those time-stamped packet data are output to the recording signal processing circuit 102a. In the recording signal processing circuit 102a, recording data comprising error correction code, ID information, sub-code, and block key information used in encrypting and the like, are generated, and a recording signal is generated,

in accordance with the recording mode determined by the control circuit 104, and recorded onto the tape 111 by the rotary head 100.

When reproducing, a reproducing operation is first performed in any reproducing mode, and ID information is detected by the reproducing signal processing circuit 102b. A determination is then made in the control circuit 104 as to which mode was recorded in, the operating mode of the reproducing signal processing circuit 102b and servo circuit 106 is reset, and reproducing is performed. In the reproducing signal processing circuit 102b, from the reproducing signal reproduced by the rotary head 100, the synchronization signal detection, error detection and correction, and the acquisition of block key information and the like are performed, and the packet data are reproduced and output to the input/output control circuit 119. In the input/output control circuit 119, packet data from which the time stamp has been removed are output to the data decryption circuit 116, referencing the timing generated by the timing generator circuit 105. In the data decryption circuit 116, the packet data are decrypted by a data key generated in the control circuit 104, based on a key generated by the device key generator 117 and a block key obtained by reproducing, and output to the input/output circuit 107.

When recording, the operational timing of the recorder-reproducer is controlled by the timing control circuit 109 based on the rate of the recording data input from the input/output terminal 108, and, when reproducing, operation is performed with a clock

signal generated by the oscillator circuit 110 as the operational reference.

Fig. 3 is a diagram of a configuration of a compressed digital video signal packet. Each packet is configured in a fixed length of, for example, 188 bytes, made up of a 4-byte packet header 306 and 184 bytes of packet information 307. The compressed digital video signal is deployed in the packet information 307 area. The packet header 307 is made up of information such as the packet information type.

Fig. 4 is a configurational diagram of the packet header 306 diagrammed in Fig. 3. Item 501 is a synchronization byte that indicates the head of the packet, 502 is an error indicator indicating whether any errors are present, 503 is a unit start indicator indicating the start of a unit, 504 is a packet priority indicating the importance of the packet, 505 is a packet ID indicating the packet type, 506 is a scrambling control indicating whether scrambling has been effected, 507 is an adaptation field control indicating whether there is added information and whether there is packet information present, and 508 is a continuity counter that is incremented in packet units.

In Fig. 5 are given diagrams of configurations of a digital broadcast transmission signal and of a signal selected from a transmission signal. Item 71 is a packet of Fig. 3. Ordinarily, an audio signal and program-related information and the like are added to the video signal noted above, and therein multiple channel programming is time-division multiplexed and transmitted.

In Fig. 5(a) is represented an example wherein 3 channels of programming are multiplexed, with V1, V2, and V3 respectively being channel video signals, and A1, A2, and A3 respectively being channel audio signal packets. In some cases, the video or audio will be configured such that there will be multiple video or audio signals on one channel. P0, P1, P2, and P3 are information relating to programs. Each respective packet is assigned a different packet ID 505 whereby the packet content can be identified.

P0 is information relating to the overall transmission signal in Fig. 5(a), wherein packets containing a program association table for recognizing which packet IDs are assigned to the respective programs, and program guide information and the like, are time-division multiplexed and transmitted. P1, P2, and P3 are information relating to the prospective programs. Therein are time-division multiplexed, and transmitted, packets including a program map table for recognizing which packet IDs have been assigned to those video packets and audio packets and the like for those channels, and scramble information and the like. Ordinarily, a predetermined value, such as 0, for example, is assigned as the program association table packet ID.

When receiving, which ID is assigned to the program map table for the program to be received is first recognized by the program association table, and, next, which IDs are assigned to the video packet and audio packet and the like by the program map table for the program to be received is recognized. Then, the video packet

and audio packet are extracted and the compressed digital data are decoded. Also, simultaneously therewith, a program clock reference is extracted, and thereby the operation of the decoder is controlled so that the compressed digital data decoding timing of the decoder is synchronized with the timing during encoding.

CR is program clock reference information for effecting synchronization when decoding the compressed digital data.

The number of multiplexed channels may be a number other than 3, of course, so there may be 4 channels, for example, and information other than that may also be multiplexed.

In Fig. 5(b), only the first channel information and program information relating thereto have been selected from Fig. 5(a). When recording the first channel, that information is output from the digital broadcast receiver 201 to the digital signal recorder-reproducer 200. Information other than that may also be included in this recording, of course, and some of the packet information may be modified to facilitate easier processing when reproducing. If the program association table information is modified to only information for a program to be recorded, for example, at reproducing time there will be no need to make a channel selection.

Fig. 6 is a configurational diagram of the data encryption circuit 115 indicated in Fig. 2. Item 1151 is a packet data input terminal, 1157 is a packet data output terminal, 1153a and 1153b are data key input terminals, 1153c is a data key selection signal input terminal, 1153d is a processing mode selection signal input terminal, 1152 and 1156 are block processing circuits, 1154 is a

key schedule circuit, 1155 is an encrypter, 1158a and 1158b are data key registers, and 1159 is a data key selector. The data encryption circuit 115 encrypts and outputs in input packet data units using a predetermined data key. When that is being done, the security of the packet data recorded on the tape can be enhanced by modifying that data key at some time interval.

The encrypter 1155 uses block encryption wherewith encryption processing can be achieved with a simple circuit configuration in units of blocks each made up of multiple bits, so that, even when an error such as a bit error occurs during transmission, that error will not affect data coming after it, that is, so that there will be no error propagation.

Packet data input from the input terminal 1151 are first divided into blocks P each made up of multiple bits in the block processing circuit 1152. Assume, for example, that one block has 64 bits. The blocks are sequentially encrypted in the encrypter 1155, as a result whereof blocks C are output, and then, in the block processing circuit 1156, the blocks are restored to the packet data format and output to the output terminal 1157. Here, the data keys that are keys for performing encryption, from the control circuit 104, are input from the data key input terminals 1153a and 1153b, and stored in the data key registers 1158a and 1158b. In the data key register 1158a, for example, the current data key is recorded, and in the data key register 1158b the next data key to be switched to is recorded.

From the data key selection signal input terminal 1153c, a signal is input, from the control circuit 104, indicating whether to select the data key in the data key register 1158a or 1158b, and the selected data key is output from the data key selector 1159. Let it be assumed here that the data key in the data key register 1158a has been selected, for example. The selected data key is converted to sub-keys KA and KB in the key schedule circuit 1154, and sent to the encrypter 1155. Assuming a data key length of 56 bits and sub-key length of 32 bits, respectively, the high order 32 bits in the data key are assigned to KA, while the added value of the high order 32 bits and low order 32 bits of the data key is assigned to KB.

Here, when modifying the data key, a signal is input from the data key selection signal input terminal 1153c so as to output the contents of the data key register 1158b, by the control circuit 104. The data key selector effects control so that, until the encryption of all of the data blocks in one packet is finished, switching is done between this and the next packet data, without switching that selection output.

In addition thereto, there is also a method of making the cipher stronger by, for example, taking the exclusive-or of the output of the encrypter 1155 and the input of the encrypter 1155 and feeding those back in block units.

Fig. 7 is a configurational diagram of the encrypter 1155 indicated in Fig. 6. In figure 7, items 551, 552, 553, and 554 are encryption processors, Pa and Pb are the upper significant and

lower significant bits in the input block data P, Ca and Cb are encrypted data, and KA and KB are sub-keys. As diagrammed in Fig. 7, the input 64-bit block P, for example, is separated into the high order 32 bits Pa and low order 32 bits Pb thereof. In the encryption processor 551, these Pa and Pb are subjected to exclusive-or processing (5511), bit shifts and addition operations (5512, 5513, 5515: A <<< p indicating that A is subjected to an end-around bit shift to the left), and adding operations (5514, 5516). The results are input to the following encryption processors 552 and 553 which perform the same processing as the encryption processor 551, and after that to an encryption processor (not shown), and multiple-stage repetitive arithmetic processing is performed. Then, from the data Ca and Cb output by the encryption processor 554 in the final stage, the encrypted block C is obtained.

In the foregoing, the data encryption circuit 115 diagrammed in Fig. 2 and Fig. 7 is described, but the encrypted block can be decrypted by performing operations in the reverse flow of the encrypter 1155, in the data decryption circuit 116. However, the operation 5516 in Fig. 7 is then made a subtraction process. For the sub-keys KA and KB, the same keys must of course be used as when encrypting.

Besides that, there are also cases where, when there is no need to protect the packet data being recorded, such as in a case where a program being recorded is permitted to be freely copied, the packet data will be recorded on the tape as it is, without being encrypted. This can be accomplished by switching the data

encryption circuit 115 and the data decryption circuit 116 from functions for encrypting and decrypting the input packets to functions that pass those packets without doing anything to them. In the data encryption circuit 115 diagrammed in Fig. 2 and Fig. 6, by fixing the input X5 going to the operation 5516 indicated in Fig. 7 to zero, by a processing mode selection signal input via the processing mode selection signal input terminal 1153d indicated in Fig. 6, although that is not diagrammed in the figures, a block can be made to pass through without performing encryption or decryption processing thereon. Based on this method, the operations can be switched while keeping the input packet processing delay time constant. There is also another method, moreover, not shown in the figures either, wherewith a switching circuit for switching to determine whether to output the packet data input from the packet data input terminal 1151 to the data output terminal 1157, without passing them through the block processing circuit 1152, encrypter 1155, or block processing circuit 1156, and whether to output the packet data output from the block processing circuit 1156 to the data output terminal 1157, is deployed in a stage in front of the data output terminal 1157, inputting the processing mode selection signal input via the processing mode selection signal input terminal 1153d to that switching circuit, and switching between packet data output from the block processing circuit 1156 and packet data input to the data output terminal 1157. These methods can be implemented also in the data decryption circuit 116

diagrammed in Fig. 2 and Fig. 19, with the same kind of configuration as described earlier.

In Fig. 8 are given diagrams of the generation of data keys in a control circuit 104 which represent cases of the generation of data keys sent to the data encryption circuit 115 and the data decryption circuit 116 indicated in Fig. 2. The device key generator 117 stores 96 bits of predetermined fixed key information, for example. The block key generator 118 is a random number generator that generates 96-bit random numbers at a command 1181 from the control circuit 104 indicated in Fig. 2, for example. Item 120 is a 96-bit exclusive-or arithmetic processor, while 121 is a hash function arithmetic processor. In Fig. 8(a), the block key and device key are made an exclusive-or by the exclusive-or arithmetic processor 120, a hash operation is performed by the hash function arithmetic processor 121, and 56 bits selected from those results are sent as a data key to the data encryption circuit 115 indicated in Fig. 2. The hash function is a function wherewith it is very difficult, from the results output thereby, to analogically infer the data input, while, from the data key, the block key and device key that are secret information cannot be found.

Also, by generating the command 1181 from the control circuit 104 indicated in Fig. 2 at some time interval, and repeatedly performing the data key generation by the operations described above, the data key can be successively modified, making it possible to enhance the security of the data on the recording medium. Next, the block key (Kr) generated by the block key

generator 118 is sent to the recording signal processing circuit 102a indicated in Fig. 2 and recorded on the tape 111.

When reproducing, the same operations as described in the foregoing are performed, but using, instead of the block key generated by the block key generator 118, a block key (Kp) reproduced from the tape 111, whereupon a data key is obtained and sent to the data decryption circuit 116 indicated in Fig. 2.

In Fig. 8(b) is represented an example where the key information Kr recorded on the tape 111 is the exclusive-or of the block key and the device key. In this case, the block key itself is input to the hash function arithmetic processor. When reproducing, the same operations as described in the foregoing are performed, but using, instead of the block key indicated in Fig. 8(a), a Kp reproduced from the tape 111, whereupon a data key is obtained and sent to the data decryption circuit 116.

The method of recording to the tape is described next.

In Fig. 9 is diagrammed a recording pattern for 1 track. Item 3 is a sub-code recording area for recording such sub-code as time information and program information, 7 is a data recording area for recording a compressed digital video signal, 2 and 6 are preambles for the respective recording areas, 4 and 8 are postambles for the respective recording areas, 5 is a gap between the respective recording areas, and 1 and 9 are margins at the edges of the tape. By providing the recording areas with postambles, preambles, and a gap, in this way, those respective areas can be independently after recorded. A digital signal other

than a compressed digital video signal may of course be recorded in the recording area 7. The data recording area 7 is configured of a plurality of blocks (which are to be distinguished from the blocks described earlier which are small encryption units).

Fig. 10 is a configurational diagram of a block in the data recording area 7 indicated in Fig. 9. Item 20 is a synchronization signal, 21 is ID information, 22 is data, and 23 is first parity (C1 parity) for detecting and correcting an error. One block is configured of 112 bytes, with the synchronization signal 20 made up of 2 bytes, the ID information 21 of 3 bytes, the data 22 of 99 bytes, and the parity 23 of 8 bytes, for example.

Fig. 11 is a configurational diagram of the ID information 21 indicated in Fig. 10. Item 31 is a group number, 32 is a track address, 33 is a block address inside 1 track, and 35 is parity for detecting error in the group number 31, track address 32, and block address 33. The block address 33 is an address for identifying a block in the recording areas. In the data recording area 7 indicated in Fig. 9, for example, that block address 33 is 0 to 335. The track address 32 is an address for identifying a track. The address is changed in 1-track or 2-track units, for example, and n tracks can be identified. By making this 0 to 5 or 0 to 2, for example, six tracks can be identified. By changing the group number 31 in Fig. 11 in 6-track units identified by the track address 32, and making it 0 to 15, 96 tracks can be identified. If the track address 32 is synchronized with the period of a second

error correction code, described subsequently, then processing when recording and identification when reproducing can be made easy.

Fig. 12 is a configurational diagram of 1 track of data in the data recording area 7 indicated in Fig. 9. Here, the synchronization signal 20 and ID information 21 indicated in Fig. 10 have been omitted. The data recording area 7 is configured of 336 blocks, for example. Data 41 are recorded in the first 306 blocks and second error correction code (C2 parity) 43 is recorded in the next 30 blocks. The C2 parity 43 is configured in n-track units, such as 6-track units, for example. Considered in 6-track units, the data are 306 blocks × 6 tracks of data. Those data are divided into 18 parts, and to each respective 102 blocks are added 10 blocks of C2 parity. For the error correction code, Reed-Solomon code may be used, for example. The 99 bytes of data in each block are configured of a 3-byte header 44 and 96 bytes of data 41.

Fig. 13 is a diagram of a configuration of blocks in 1 packet when a compressed digital video signal transmitted in a 188-byte packet format is recorded in the data 41 indicated in Fig. 12. In this case, 4 bytes of time stamp information 25 are added to make 192 bytes, and 1 packet is recorded in 2 blocks. The time stamp information 25 is information on the time a packet was transmitted. More specifically, the time when the head of a packet was transmitted or the interval between packets is counted with a reference clock signal, that count value is recorded together with the packet data, and the interval between packets is set, based on

that information, when reproducing. When that is done, data can be output in the same interval as when transmitted.

Fig. 14 is a configurational diagram of the header 44 in the data recording area 7 indicated in Fig. 12. This header 44 is configured of format information 45, block information 46, and auxiliary information 47. In the format information 45 and block information 46 are recorded various kinds of recording information relating to recording, while in the auxiliary information 47 is recorded other supplemental information.

The format information 45 is information relating to the recording format, and configures one item of information with multiple blocks, containing the recording mode (identifying a standard speed mode and other things), the type of packet data handled, and copy control information indicating whether or not the packet data recorded can be copied, etc. One item of information is configured in 12 bytes of 12 blocks, for example. By repeating this information a plural number of times and multiply recording it, moreover, the detection capability when reproducing is enhanced. It is also possible to record the key information and the like described earlier here.

The block information 46 is information for identifying the type of data recorded in the data recording area 41. Here are recorded whether or not there are high-speed variable-speed reproducing data and the type thereof (indicating to which speed the high-speed variable-speed reproducing data correspond to), etc.

It is also possible to record the key information and the like described earlier here.

The auxiliary information 47 configures pack data that are one item of information in 6 bytes of 6 blocks. By making the first byte an item code representing the information type, and the remaining 5 bytes data, various kinds of data can be recorded. Key information such as the block key described earlier, or other information, such as information on recording time and the like, or the type of recording signal or the like, for example, can be recorded here.

Fig. 15 is a diagram of a configuration for pack data when block keys are held in the added information 47 area indicated in Fig. 14.

In the first byte of the pack data is held an item code indicating that the information which follows is key information.

In the second byte, information indicating the type of key that is held (key sequence number, key attribute, or key flag) is recorded. As described earlier, the security of the data on the recording medium can be enhanced by successively modifying the block key at some time interval, wherefore, key attribute information is recorded to indicate whether the block key held in this pack is the block key used in encrypting the current packet data or the block key to be used next. Also, the switching timing is recorded with a key flag that reverses every time the block key is updated. With this information, the switching of keys when reproducing is made smooth. In the key sequence number, moreover,

when the block key cannot be held in 1 pack, information is held which indicates that there is a following pack. When the block key is 96 bits, for example, it is divided and held in 3 packs, with 2, 1, and 0, respectively, held in each key sequence number, where the 0 indicates that that is the last pack. In addition, there is also the method of storing the size of all the data so that the size of what remains may be known.

The block key is contained from the 3rd to the 6th byte.

In the example diagrammed in Fig. 8(b), described earlier, the key information Kp is held instead of the block key.

Fig. 16 is a diagram of a block key holding method. In the case represented in this example, only the current key information is recorded in the pack data in each track. Accordingly, the key attribute described earlier is fixed information that only indicates the current key, and need not be recorded. In (1) in Fig. 16 is diagrammed a condition where a 96-bit current block key A (A0 to A11) is divided and held in 3 packs. Ordinarily, these packs are recorded a plurality of times, for 1 track, in order to enhance data reliability. By recording 3 packs in a first, middle, and last area, respectively, in a track (making a total of 9), for example, the effects of reproducing signal dropouts caused by magnetic head clogging and the like can be reduced. Also, there is no absolute necessity of recording 3 packs as consecutive packs, but, by inserting packs holding other information between packs, and recording the packs holding the key information so that they are dispersed, it becomes possible to protect the key information

itself and further enhance reliability. At (2) in Fig. 16 are diagrammed pack data recorded in a track where the block key has been switched to B. In this case, the key flag for the block key B is reversed.

Fig. 17 is a diagram of another block key holding method. In the method represented in Fig. 17, the key information to be used next is pre-generated and recorded along with the current key information. Here, the key attribute information is made "0" for a block key that is being used in encrypting the current packet data and "1" for the block key that will be used next. Also, the key flag that reverses every time the block key is updated alternates repeatedly between "0" and "1."

In (1) in Fig. 17 is diagrammed a condition where a 96-bit current block key A is held. In (2), the next block key B is held. The (1) and (2) here are recorded in the added information area in a block in the same track. (3) are pack data recorded in a track where the block key has been switched to B. In this case, the block key B has reverted to the current key having key attribute information "0," and the key flag is also reversed. And in (4), the key C to be used next is held. (3) and (4) are recorded in a track as pack data in the same track.

In terms of the location where the key flags are held that indicate block key update timing, instead of holding those in an added information 47 pack, there is the method of holding them in the format information 45 or block information 46 diagrammed in Fig. 14, described earlier.

As noted earlier, the key information is recorded on the tape. However, by using the points of separation between each n tracks (6 tracks in this embodiment) that is the unit for adding the C2 parity described earlier for the timing wherewith the block key is switched, C2 parity operations become possible, when reproducing, and the data reliability of key information is enhanced.

In the example described in the foregoing, moreover, information indicating the timing wherewith the block key is updated is recorded as a key flag. However, by synchronizing the C2 parity operation period and update timing with the value of the track address 32 or group number 31 indicated in Fig. 11 and described earlier, in the recording signal processing circuit 102a indicated in Fig. 2, it is possible also to detect the key information update timing when reproducing with the value of that track address 32 or group number 31. In the recording signal processing circuit 102a, for example, the track address 32 repeats the values of 0 to 5 for each track, and the 6 tracks of those values 0 to 5 are made the unit of adding the C2 parity described earlier. Then, with timing wherewith the value goes from 5 to 0, in the data encryption circuit 115, the block key is updated, and recorded. When reproducing, it is only necessary to detect the timing wherewith the value of that track address 32 goes from 5 to 0, in the reproducing signal processing circuit 102b indicated in Fig. 2, and go on updating the key in the data decryption circuit 116. Also, in cases where update is done with an even longer period, it is possible to detect the update timing in 96-track

units, and at the points of separation between the units wherewith the C2 parity is added, using the group number 31, by incrementing the group number 31, when the value of the track address 32 goes from 5 to 0, making provision so that the values from 0 to 15 are repeated.

Fig. 18 is a diagram of a specific configuration for the time stamp information 25 (4 bytes = 32 bits) indicated in Fig. 13, representing another method for holding a key flag and encryption flag. In the example diagrammed here, the time stamp information 251 is 22 bits of information, item 252 is the key flag (1 bit) described earlier, and 253 is a encryption flag (1 bit) indicating whether the following packet data are encrypted or not. When recording, the input/output control circuit 119 indicated in Fig. 2, together with time stamp information 251 that is a time stamp, places a "1," for example, in the encryption flag 253 when the following packet data are encrypted, and a "0" therein when not encrypted, and, in the key flag 252, places the key flag for the pack data holding the key information described earlier that corresponds to the following packet data. When reproducing, in the input/output control circuit 119 indicated in Fig. 2, the time stamp information 25 added when recording is removed and output to the data decryption circuit 116, and, together therewith, the encryption flag 253 and the key flag 252 are sent to the data decryption circuit 116, and the operation of the data decryption circuit 116 is controlled.

Fig. 19 is a configurational diagram of the data decryption circuit 116 indicated in Fig. 2. Item 1161 is a packet data input terminal, 1167 is a packet data output terminal, 1163a and 1163b are data key input terminals, 1163c is a data key input terminal, 1163c is a data key selection signal input terminal, 1163d is a processing mode selection signal input terminal, 1162 and 1166 are block processing circuits, 1164 is a key schedule circuit, 1165 is a decrypter, 1168a and 1168b are data key registers, and 1169 is a data key selector. The data decryption circuit 116 decrypts, and outputs, in units of the packet data input, using predetermined data keys.

The decrypter 1165 uses block cipher to effect decryption processing in units of blocks configured of multiple bits.

The packet data input from the input terminal 1161 are divided into blocks C made up of multiple bits, in the same manner as with the data encryption circuit 115. The blocks are sequentially decrypted in the decrypter 1165, as a result whereof blocks P are output, and then, in the block processing circuit 1166, the blocks are restored to the packet data format and output to the output terminal 1167. Here, the data keys that are keys for performing decryption, from the control circuit 104, are input from the data key input terminals 1163a and 1163b, and stored in the data key registers 1168a and 1168b. In the data key register 1168a, for example, the current data key is recorded, and in the data key register 1168b the next data key to be switched to is recorded.

Furthermore, from the processing mode selection signal input terminal 1163d, the detected encryption flag 253 from the input/output control circuit 109 is input, and either a mode for a decrypting operation or a mode for passing the data without doing anything is determined. From the data key selection signal input terminal 1163c, moreover, the detected key flag 252 is input from the input/output control circuit 109, and the selected data key is output by the data key selector 1169. The selected data key is converted in the schedule circuit 1164 to sub-keys KA and KB and sent to the encrypter 1165.

Here, when the encryption flag or key flag detected by the input/output control circuit 119 indicated in Fig. 2 changes, in conjunction therewith, the operating mode of the data decryption circuit 116 and the data key are selected.

As described in the foregoing, by adding the encryption flag or key flag to the packet data, whether or not encryption has been done, and key information, can be determined, and decryption processing effected, in packet data units.

In terms of the location where the encryption flag indicating whether or not encryption has been done is held, there is the method of holding that in the second byte in the pack holding the key information indicated in Fig. 15, and, alternatively, the method of holding it in the format information 45 or block information 46 indicated in Fig. 14, as described earlier.

By holding the encryption flag in the format information 45 or block information 46 or the like, and making provision so that,

when the encryption flag indicates "1," for example, that is, when the packet data are encrypted, the operation of the data decryption circuit 116 is made the decryption operation and so that key information is fetched from the pack holding the key information in the added information 47, and, when the encryption flag is "0," so that the operation of the data decryption circuit 116 is made to output as is without decrypting, control operations when packet data are not encrypted can be simplified. With the method of holding the encryption flag in the pack holding the key information, moreover, when the encryption flag is "0," that is, when the packet data are not encrypted, block key information from the third byte on in that pack is not held.

In addition, whether or not encryption has been done can be determined by whether or not there is a pack holding key information, for example, without using the encryption flag.

Fig. 20 is a configurational diagram of a digital recording and reproducing signal processing circuit 102 that comprises the recording signal processing circuit 102a and the reproducing signal processing circuit 102b indicated in Fig. 2. Item 400 is a memory circuit, 401 is a memory control circuit for generating addresses and the like for controlling the memory circuit 400 in subordination to the control circuit 104 indicated in Fig. 2, 402 is a C2 parity arithmetic processing circuit, 403 is a C1 parity arithmetic processing circuit, 404 is an auxiliary information processing circuit for adding auxiliary information when recording, according to content set from the control circuit 104, such as ID

information, sub-code generation information, format information, block information, and key information, and for fetching auxiliary information when reproducing, such as ID information, sub-code, format information, block information, and key information, etc., and 405 is a modulation/demodulation circuit for performing modulation processing when recording and demodulation processing when reproducing. In this embodiment, as one example, 6 tracks of data are required in order to perform a C2 parity operation, wherefore the memory circuit 400 is to have sufficient capacity to store at least 6 tracks of data.

When recording, a recording state is set via the terminals 411 and 413 by the control circuit 104 indicated in Fig. 2. The packet data encrypted by the data encryption circuit 115 indicated in Fig. 2 are input from the terminal 410, and accumulated in the memory circuit 400 in accordance with control signals from the memory control circuit 401. After the data required for the C2 parity operation have been accumulated, they are sequentially read out from the memory circuit 400 and input to the C2 parity arithmetic processing circuit 402, and the prescribed arithmetic operation is performed. The operational results obtained by the C2 parity arithmetic processing circuit 402 are accumulated in the memory circuit 400. Meanwhile, in the auxiliary information processing circuit 404, in accordance with settings from the control circuit 104 via the terminal 413, packet data such as key information corresponding to the key of the input encrypted packet data are generated, and accumulated in the memory circuit 400.

Then, as when configuring the recording blocks described earlier, the data read out from the memory circuit 400 containing the key information and the like have C1 parity added thereto by the C1 parity arithmetic processing circuit 403 and are input to the modulation/demodulation circuit 405. The signal, subjected to prescribed modulation processing by the modulation/demodulation circuit 405, is output via the terminal 414,and is recorded on the tape 111 by the rotary head 100 indicated in Fig. 2.

Fig. 21 is a timing chart for signal processing when data recording is started. Packet data input from the data encryption circuit 115 are diagrammed in Fig. 21(a), the data key used by the data encryption circuit 115 when encrypting in Fig. 21(b), the C2 parity operation cycle (6 tracks in this embodiment) performed by the C2 parity arithmetic processing circuit 402 indicated in Fig. 20, together with the six-track unit configuration of the C2 parity 43 described earlier, in Fig. 21(c), and the recording signal recorded through the rotary head 100 onto the tape 111 in Fig. 2(d). In the embodiment diagrammed in Fig. 21, the block key A is generated beforehand, and the data key Ka is calculated and sent to the data encryption circuit 115, prior to the time t1 for which recording start is set. Control is also effected so that, prior to the time t1 for which the recording start is set, the recording signal processing circuit 102a judges that there is no packet, irrespective of the input signal, and performs recording signal processing. Thus, even when the recording start is set to the time

t0, it will be possible to perform C2 parity operations on the data in the time period p0.

The control circuit 104 indicated in Fig. 2 effects control so that the C2 parity operation cycle S0 for the data input when recording started at time t0 ends, and the recording signal is output from the head of n tracks (6 tracks in this embodiment) that configure the second error correction code noted earlier (Fig. 21(d)). The data key, moreover, is updated in this C2 parity operation cycle. For example, the block key B is generated prior to time t2, the data key Kb is calculated and sent ahead to the data encryption circuit 115, and, at time t2, the data key is switched to Kb in the data encryption circuit 115. Ordinarily, in the data encryption circuit 115, in order to perform that process, a delay time occurs, from the input of the packet data to the output thereof. That being the case, at a point in time that is earlier by the measure of the data delay that occurs from the time t2 due to the packet encryption processing performed by the data encryption circuit 115, the data key sent to the data encryption circuit 115 is switched to Kb. Alternatively, data from the packet data for which the data key was switched may be sent ahead to the processing in the next arithmetic operation cycle. In this embodiment, extra data are recorded in the head portion, but C2 parity can be added to the signal to be recorded, irrespective of the timing at time t1 at which recording is to start, and recording done in units of the C2 parity operation cycle described above. When reproducing, moreover, the extra data portion at the head will

is only used in the C2 parity calculation, and is never output, because recording processing is done assuming no packet.

When recording is finished, the recording operation to the tape 111 of the recording signal processing circuit 102a is controlled by the control circuit 104 so that it is performed at the completion of the arithmetic operation cycle (6 tracks in this embodiment) for calculating the C2 parity using multiple track data. With this control scheme, irrespective of the recording start and recording end switching timing, C2 parity is added to all recorded data on the tape 111, and key information is updated and the packet data are encrypted in C2 parity operation cycle units, wherefore, when reproducing, reproduction can be done in C2 parity operation cycle units, and C2 parity calculations become possible, wherefore the key information data reliability is enhanced also.

Fig. 22 is a diagram of key information in the tape 111 indicated in Fig. 2. In this figure, items 1111 to 1117 are recording tracks represented in units of 6 tracks which is the C2 parity operation cycle. In the case diagrammed in Fig. 22, recording tracks 1111 to 1113 hold packet data encrypted using the block key A and recording tracks 1114 to 1116 hold packet data encrypted using the block key B, together with pack data that constitute key information corresponding thereto, respectively. The recording track 1117 is a track that is recorded without being encrypted. It is possible to have tracks that are encrypted and tracks that are not encrypted mixed together on the same tape, as diagrammed here. It is conceivable that key information update be

done once every m × n tracks (where m is an integer 1 or greater and n, in this embodiment, is 6), such as every 48 tracks or every 96 tracks, or, alternatively, for one entire program or the like. However, the point of key switching, or the boundary between an encrypted track and an unencrypted track, is the point where C2 parity operation cycles (6 tracks in this embodiment) are separated.

The operations when recording have been described in the foregoing. It is also possible here to record key information in the sub-code areas (7 in Fig. 9). However, when key information is held in the header (44 in Fig. 12) portion of each block and recording is done in the data recording areas (7 in Fig. 9) on the tracks, it becomes very difficult to rewrite only the key information by dubbing or the like. That being so, loss of key information can be prevented, and a benefit is gained in that deliberate efforts to alter only the key information and intentionally perform cryptic communication cannot succeed.

Next, the method of reproducing from tape is described.

In the digital recording and reproducing signal processing circuit 102 diagrammed in Fig. 20, when reproducing, a reproducing state is set by the control circuit 104 indicated in Fig. 2 via the terminals 411 and 413. The reproducing signal that is reproduced from the tape 111 by the rotary head 100 and input from the terminal 414 is subjected to demodulation processing by the modulation/demodulation circuit 405, then to a C1 parity operation by the C1 parity arithmetic processing circuit 403, whereupon the detection and correction of errors are performed, and the results

of the C1 parity operation also are accumulated together in the memory circuit 400. After the data required for the C2 parity operation have been accumulated, those data are sequentially read out from the memory circuit 400, in accordance with control signals of the memory control circuit 401, and input to the C2 parity arithmetic processing circuit 402. In the C2 parity arithmetic processing circuit 402, arithmetic operations are performed with the data noted above, and the data that have been subjected to error detection and correction processing are again accumulated, together with the results of the C2 parity operation, in the memory circuit 400.

Data are read out from the memory circuit 400 in a prescribed order, referenced to a timing signal input via the terminal 412 from the timing generator circuit 105 indicated in Fig. 2, the C1 parity and C2 parity operation results described earlier are referenced, and only errorless data are output from the terminal 410 to the input/output control circuit 119. In the auxiliary information processing circuit 404, meanwhile, key information and sub-codes and the like are acquired from data read out from the memory circuit 400, and sent via the terminal 413 to the control circuit 104 indicated in Fig. 2. Then, the operations diagrammed in Fig. 8 are performed, that is, Kp is extracted from the key information obtained by generation, the exclusive-or with the device key obtained from the device key generator 117 is taken, the operation of the hash function arithmetic processor 121 is performed, and a data key is obtained and output to the data

decryption circuit 116 indicated in Fig. 2. This data key is identical to the data key used when recording, and therewith, in the data decryption circuit 116, the original packet data can be obtained accurately.

Fig. 23 is a timing chart for signal processing when reproducing data in the present invention. A reproducing signal reproduced from the tape 111 via the rotary head 100 is diagrammed in Fig. 23(a), the C2 parity operation cycle (6 tracks in this embodiment) described earlier is diagrammed in Fig. 23(b), packet data output from the input/output control circuit 119 is diagrammed in Fig. 23(c), and a data key sent to the data decryption circuit 116 indicated in Fig. 2 is diagrammed in Fig. 23(d). In the auxiliary information processing circuit 404, in the operation cycle s3, the key information KpC used in this cycle is detected. By this Kpc, the data key Kc obtained by the operation described earlier is stored in the data key register 1163a described earlier, for example, and the data key selector 1169 is also selected so that the data key Kc in the data key register 1163a is output.

Next, in the operation cycle s4, when it is detected that the key information KpD is being used, a data key Kd is derived ahead of time, by the previously described operation, and stored in the data key register 1163b, and, timed to the time t3, the data key selector 1169 is operated and the data key Kd in the data key register 1163b is switched to. Using the method described above, it is possible to perform a reproducing operation while updating the data key.

Furthermore, when making an additional recording to an already recorded tape, by providing so that the recording is started from a point of separation between C2 parity addition units, add-on recording is made possible without impairing the data reliability of the track key information immediately prior to the additional recording.

Besides that, in terms of a method for distinguishing whether or not packet data have been encrypted, because the synchronization byte 501 indicated in Fig. 4 ordinarily consists of fixed data, that synchronization byte may be detected for in the reproducing signal processing circuit 102b, for example, and, when such can be detected, the data decryption circuit 116 indicated in Fig. 2 switched to a function that passes packet data input thereto without doing anything to it, but, when the synchronization byte cannot be detected, switching the data decryption circuit 116 indicated in Fig. 2 to decryption function operation, and performing an operation to detect key information in the added information area. By so doing, when recording, detection will be possible, even with tape wherein tracks on which packet data are encrypted and recorded and tracks on which packet data are recorded without being encrypted coexist together.

Furthermore, even with prerecorded software tape, the production and reproducing of software tape is made possible with the method described in the foregoing, and the protection of packet data on such tape can be realized.

In the examples described in the foregoing, the current block key is held in a recording track, but the data key calculation must be performed in a single C2 arithmetic operation cycle. In a case where the data key calculation cannot be done quickly enough, within a single C2 arithmetic operation cycle, then, by recording the current block key and the next block key in a recording track, as described earlier, the next data key will be found ahead of time.

Fig. 24 is a diagram of another configuration of the digital signal recorder-reproducer 200 indicated in Fig. 1. In this figure, item 121 is a digital interface circuit that effects a protocol such as a high-speed digital bus interface such as IEEE 1394, for example. This digital interface circuit 121 has functions for transmitting data at high speed while maintaining the time intervals in the input packet data. Item 122 in Fig. 24 is a digital interface bus. Item 123 is an encryption/decryption circuit for protecting digital data transmitted over the digital interface 122. This circuit 123 either encrypts packet data and transmits those encrypted data over the digital interface bus 122, or decrypts received digital data. Item 124 is a control circuit, such as a microprocessor, for controlling the digital interface circuit 121 and the encryption/ decryption circuit 123.

When recording, encrypted digital data that come transmitted in over the digital interface bus 122 are subjected to prescribed packet processing in the digital interface circuit 121, then, in the encryption/decryption circuit 123, decrypted to the original packet data and output to the input/output circuit 107. After that,

as described earlier, the packet data are encrypted in the data encryption circuit 115 and recorded on the tape 111. When reproducing, in the data decryption circuit 116, reproduced packet data are decrypted, output from the input/output circuit 107 to the encryption/decryption circuit 123, encrypted in the encryption/decryption circuit 123, and output from the digital interface circuit 121 to the digital interface bus 122. Based on this, the protection both of packet data on a tape and of packet data on a digital interface bus can be realized.

In the embodiment described in the foregoing, moreover, recording on and reproducing from a tape are described, but the present invention can be similarly applied when recording on and reproducing from a disk such as an optical disk or magnetic disk, a semiconductor memory or the like, or any other recording medium.

In the case of the disks noted above, key information switching, or the switching to determine whether or not to perform encryption, may be performed at the points of separation between sectors, which are one unit of recording on a disk.

Also, in the case of the semiconductor memory noted above, key information switching, or the switching to determine whether or not to perform encryption, may be performed at the points of separation between addresses, which are one unit of recording on a semiconductor memory.

This embodiment, moreover, is one that is applied to a system for encrypting a digital signal using a key. The present invention is not limited to or by this embodiment, however, and can be

applied also to systems wherein a digital signal is scrambled or the like using a key code. In other words, the present invention can be applied to all systems wherein a digital signal is processed so that it is converted from its original clear state.

According to the present invention, in a digital signal recorder, reproducer, and recording medium, wherewith recording is done on or reproducing is done from the recording medium, when recording, key information is subjected to a prescribed operation to yield a key, the digital signal is encrypted, and recorded together with the key information onto the recording medium, whereas, when reproducing, the key information reproduced from the recording medium is subjected to the prescribed operation, and, with the key obtained thereby, the reproduced digital signal is decrypted and output. Based on the foregoing, when reproducing, so long as the prescribed operation is not performed, the key cannot be obtained. Therefore, even though the key information on the recording medium be obtained, it is very difficult, using that information, to decrypt the encrypted digital signal. Thus the copyrights of the digital signal on the recording medium can be protected.

CLAIMS:

1. A digital signal recorder for recording a digital signal on a recording medium, comprising:

key information generation means for generating at least one item of key information;

key generation means which receive said key information and perform a prescribed arithmetic operation thereon and generate a key;

an encryption circuit which receives said key and said digital signal and encrypts said digital signal with said key and outputs the resulting encrypted digital signal; and

a recording circuit which records at least one of said items of key information, together with said encrypted digital signal, in prescribed area on said recording medium.

2. The digital signal recorder according to claim 1, characterized in that said digital signal has a packet format of a prescribed length.

3. The digital signal recorder according to claim 1, characterized in that:

said key information generation means have a function for updating at least one item of said key information at a prescribed time interval; and

said recording circuit has a function for recording information capable of identifying timing wherewith said key information generation means update said key information, in prescribed area on said recording medium.

4. The digital signal recorder according to claim 3, characterized in that:

said digital signal has a packet format of a prescribed length; and

said recording circuit has a function for adding information capable of identifying timing wherewith said key information generation means update said key information to packets of said digital signal and recording on said recording medium.

5. The digital signal recorder according to claim 1, characterized in that:

said encryption circuit further has a function capable of selecting between a function for encrypting and outputting said digital signal and a function for outputting said digital signal as is without encryption; and

said recording circuit has a function for recording, in prescribed area on said recording medium, encryption flag information indicating whether or not said digital signal is encrypted, and, when not encrypted, not recording said key information.

6. The digital signal recorder according to claim 5, characterized in that:

said digital signal has a packet format of a prescribed length; and

said recording circuit has a function for adding encryption flag information indicating whether or not said digital

signal is encrypted, to packets of said digital signal, and recording on said recording medium.

7. A digital signal recorder in which a digital signal of a packet format of a prescribed length is input and divided into other prescribed lengths; a synchronization signal, recording information signal, auxiliary information signal, and first error correction code are added thereto to define a block format; one track is formed by a prescribed number of blocks thus made; a second error correction code is added in units of n tracks (where n is an integer 1 or greater); said second error correction code is also divided and said first error correction code is added thereto to constitute a block format; and said tracks are recorded on said recording medium; comprising:

key information generation means for generating at least one item of key information;

key generation means which receive said key information and perform a prescribed arithmetic operation to generate a key;

an encryption circuit which receives said key and said digital signal, encrypts said digital signal with said key and outputs the resulting encrypted digital signal; and

a recording circuit which records at least one of said items of key information, together with said encrypted digital signal, in prescribed area on said recording medium.

8. The digital signal recorder according to claim 7, characterized in that said recording circuit has a function for

holding said key information in an auxiliary information signal area in said blocks and recording same on said recording medium.

9. The digital signal recorder according to claim 7, characterized in that: said key information generation means have a function for updating at least one item of said key information at a prescribed time interval; and said recording circuit has a function for recording information capable of identifying timing wherewith said key information generation means update said key information, in prescribed area on said recording medium.

10. The digital signal recorder according to claim 9, characterized in that said recording circuit has a function for holding said information capable of identifying said timing in a recording information signal area in said blocks and recording same on said recording medium.

11. The digital signal recorder according to claim 9, characterized in that said recording circuit has a function for holding said information capable of identifying said timing in an auxiliary information signal area in said blocks and recording same on said recording medium.

12. The digital signal recorder according to claim 9, characterized in that said recording circuit has a function for adding said information capable of identifying said timing to packets in said digital signal and recording same on said recording medium.

13. The digital signal recorder according to claim 9, characterized in that said key information generation means have a

function for updating said key information at points of separation between units of n tracks wherewith said second error correction code was added.

14. The digital signal recorder according to claim 7, characterized in that:

said encryption circuit has a function for encrypting and outputting said digital signal; and a function for outputting same as is, without encryption; and

said recording circuit has a function for recording encryption flag information indicating whether or not said digital signal is encrypted, in prescribed area on said recording medium, and, when not encrypted, not recording said key information.

15. The digital signal recorder according to claim 14, characterized in that said recording circuit has a function for holding said encryption flag information in recording information signal area of said blocks and recording same on said recording medium.

16. The digital signal recorder according to claim 14, characterized in that said recording circuit has a function for holding said encryption flag information in auxiliary information signal area of said blocks and recording same on said recording medium.

17. The digital signal recorder according to claim 14, characterized in that said recording circuit has a function for adding said encryption flag information to packets in said digital signal.

18. The digital signal recorder according to claim 14, characterized in that said encryption circuit has a function for switching to determine whether or not to encrypt said digital signal, at points of separation between units of n tracks wherewith said second error correction code was added.

19. A digital signal reproducer for reproducing a digital signal recorded on a recording medium, comprising:

a reproducing circuit which reproduces at least one item of key information recorded in prescribed area on said recording medium, and said digital signal;

key generation means which receive said key information and perform a prescribed arithmetic operation thereon to generate a key; and

a decryption circuit which receives said key and said reproduced digital signal and decrypts said digital signal with said key.

20. The digital signal reproducer according to claim 19, characterized in that said digital signal has a packet format of a prescribed length.

21. The digital signal reproducer according to claim 19, characterized in that:

key information generation means are provided for generating at least one other item of key information; and

said key generation means comprises a function for receiving key information and said other key information, and performing a prescribed arithmetic operation to generate a key.

22. The digital signal reproducer according to claim 19, characterized in that:

said reproducing circuit has a function for reproducing said key information that has been updated, and information capable of identifying timing wherewith said key information is updated, recorded in prescribed area on said recording medium;

said key generation means have a function for receiving at least said updated key information, and for performing a prescribed arithmetic operation to generate a updated key; and

said decryption circuit comprises a switching circuit which switches said key that has been input, to said updated key in coordination with said timing signal.

23. The digital signal reproducer according to claim 22, characterized in that said digital signal has a packet format of a prescribed length; and said reproducing circuit has a function for reproducing information capable of identifying said timing, which information has been added to packets in said digital signal and recorded.

24. The digital signal reproducer according to claim 19, characterized in that:

said reproducing circuit has a function for reproducing encryption flag information indicating whether or not said digital signal is encrypted, which information is recorded in prescribed area on said recording medium; and

said decryption circuit has a function for selecting and switching between a function for decrypting, and outputting,

said digital signal that was reproduced, and a function for outputting said digital signal as is, without decryption, according to said encryption flag information.

25. The digital signal reproducer according to claim 24, characterized in that:

said digital signal has a packet format of a prescribed length; and

said reproducing circuit has a function for reproducing encryption flag information indicating whether or not said digital signal is encrypted, which information has been added to packets in said digital signal and recorded,.

26. A digital signal reproducer in which a digital signal of a packet format of a prescribed length is input and divided into other prescribed lengths; a synchronization signal, recording information signal, added information signal, and first error correction code are added thereto to define a block format; one track is formed by a prescribed number of blocks thus made; a second error correction code is added in units of n tracks (where n is an integer 1 or greater); said second error correction code is also divided and said first error correction code is added thereto to constitute a block format; and said digital signal recorded on said recording medium is reproduced; said digital signal recorder being characterized by comprising:

a reproducing circuit which reproduces at least one item of key information recorded in prescribed area on said recording medium, and said digital signal;

key generation means which receive said key information and perform a prescribed arithmetic operation to generate a key; and

a decryption circuit which receives said key and said reproduced digital signal, decrypts said digital signal with said key and outputs the decrypted signal.

27. The digital signal reproducer according to claim 26, characterized by further comprising key information generation means for generating at least one item of other key information; and characterized in that said key generation means have a function for receiving said key information and said other key information, and performing a prescribed arithmetic operation to generate a key.

28. The digital signal reproducer according to claim 26, characterized in that said reproducing circuit have a function for reproducing said key information recorded in auxiliary information signal area in said blocks on said recording medium.

29. The digital signal reproducer according to claim 26, characterized in that:

said reproducing circuit has a function for reproducing said key information that has been updated, and information capable of identifying timing wherewith said key information is updated, recorded in prescribed area on said recording medium;

said key generation means have a function for receiving at least said updated key information and performing a prescribed arithmetic operation to generate an updated key; and

said decryption circuit comprises a witching circuit which switches said key that has been input, to said updated key in coordination with said timing signal.

30. The digital signal reproducer according to claim 29, characterized in that said reproducing circuit has a function for reproducing information capable of identifying said timing, which information is recorded in recording information signal area in said blocks.

31. The digital signal reproducer according to claim 29, characterized in that said reproducing circuit has a function for reproducing information capable of identifying said timing, which information is recorded in auxiliary information signal area in said blocks.

32. The digital signal reproducer according to claim 29, characterized in that said reproducing circuit has a function for reproducing information capable of identifying said timing, which has been added to packets in said digital signal and recorded.

33. The digital signal reproducer according to claim 29, characterized in that said reproducing circuit has a function for reproducing said key information, which information is updated at points of separation between units of n tracks wherewith said second error correction code was added.

34. The digital signal reproducer according to claim 26, characterized in that:

said reproducing circuit has a function for generating encryption flag information indicating whether or not said digital

signal is encrypted, recorded in prescribed area on said recording medium; and

said decryption circuit has a function for selecting and switching between a function for decrypting, and outputting, said digital signal that has reproduced, and a function for outputting said digital signal as is, without decryption, according to said encryption flag information.

35. The digital signal reproducer according to claim 34, characterized in that said reproducing circuit has a function for reproducing encryption flag information indicating whether or not said digital signal is encrypted, which information is recorded in recording information signal area in said blocks.

36. The digital signal reproducer according to claim 34, characterized in that said reproducing circuit has a function for reproducing encryption flag information indicating whether or not said digital signal is encrypted, which information is recorded in auxiliary information signal area in said blocks.

37. The digital signal reproducer according to claim 34, characterized in that said reproducing circuit has a function for reproducing encryption flag information indicating whether or not said digital signal is encrypted, which information has been added to packets in said digital signal and recorded.

38. The digital signal reproducer according to claim 34, characterized in that said reproducing circuit has a function for reproducing said encryption flag information, which is switched at

points of separation between units of n tracks wherewith said second error correction code was added.

39. A digital recording medium having a digital signal recorded thereon, characterized in that:

said digital signal, encrypted with a key obtained by performing a prescribed arithmetic operation on key information, is recorded, together with said key information, in prescribed area.

40. The digital signal recording medium according to claim 39, characterized in that said digital signal has a packet format of a prescribed length.

41. The digital signal recording medium according to claim 39, characterized in that said key information is updated at a prescribed interval and recorded in prescribed area.

42. The digital signal recording medium according to claim 39, characterized in that information capable of identifying timing indicating that said key information was updated at a prescribed interval is recorded in prescribed area.

43. The digital signal recording medium according to claim 39, characterized in that: encryption flag information indicating whether or not said digital signal is encrypted is recorded in prescribed area; and, when said digital signal is not encrypted, said key information is not recorded.

44. A digital signal recorder, comprising:

key generation means for generating a plurality of types of keys for converting a digital signal;

a conversion circuit which converts said digital signal using said keys and outputs the converted digital signal after conversion; and

a recording circuit which records said keys and said converted digital signal on a recording medium.

45. A digital signal reproducer wherein a medium on which are recorded a converted digital signal converted with a plurality of types of keys, and said keys, is used; and said digital signal reproducer comprising:

a reproducing circuit which reproduces, and outputs, said converted digital signal and said keys, from said medium; and

a de-conversion circuit, to which is input the output from said reproducing circuit, which de-converts said converted digital signal using said keys.

46. A recording medium whereon a converted digital signal converted with a plurality of types of keys, and said keys, are recorded.

ABSTRACT OF THE DISCLOSURE

A recorder, producer, and recording medium, wherewith the copyrights of digital signals on the recording medium can be protected, are disclosed. In a digital signal recorder and reproducer for recording or reproducing a digital signal, on a recording medium, and a recording medium, when recording, the digital signal is encrypted with a key obtained by subjecting key information to a prescribed arithmetic operation, and recorded, together with the key information, on the recording medium, whereas, when reproducing, the reproduced digital signal is decrypted with a key obtained by subjecting the key information reproduced from the recording medium to the prescribed arithmetic operation, and output.

FIG.1

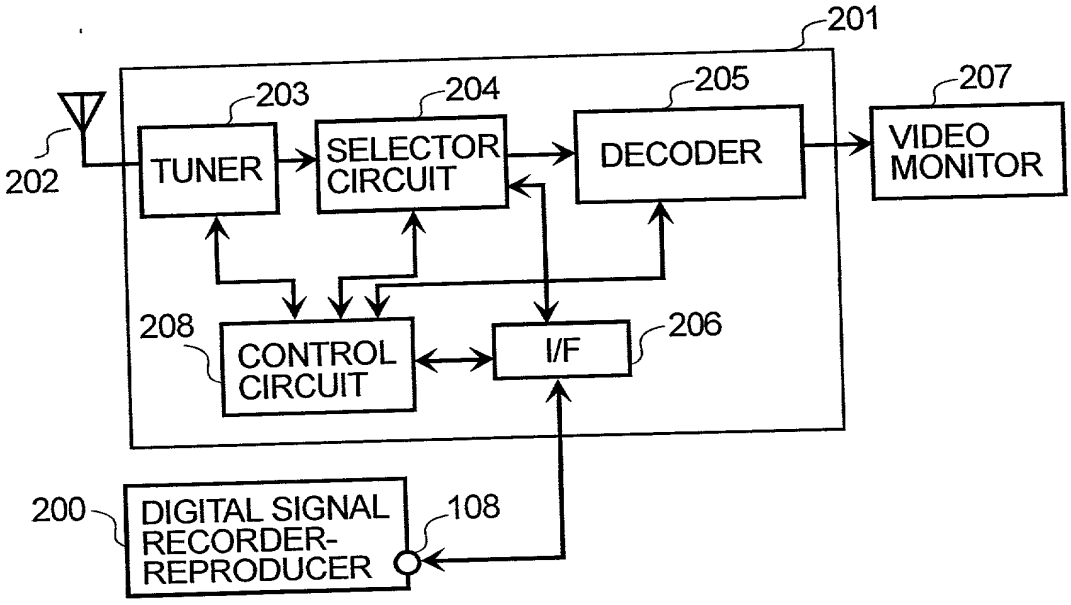

201
202
203
TUNER
204
SELECTOR CIRCUIT
205
DECODER
207
VIDEO MONITOR
208
CONTROL CIRCUIT
I/F
206
200
DIGITAL SIGNAL RECORDER-REPRODUCER
108

FIG.2

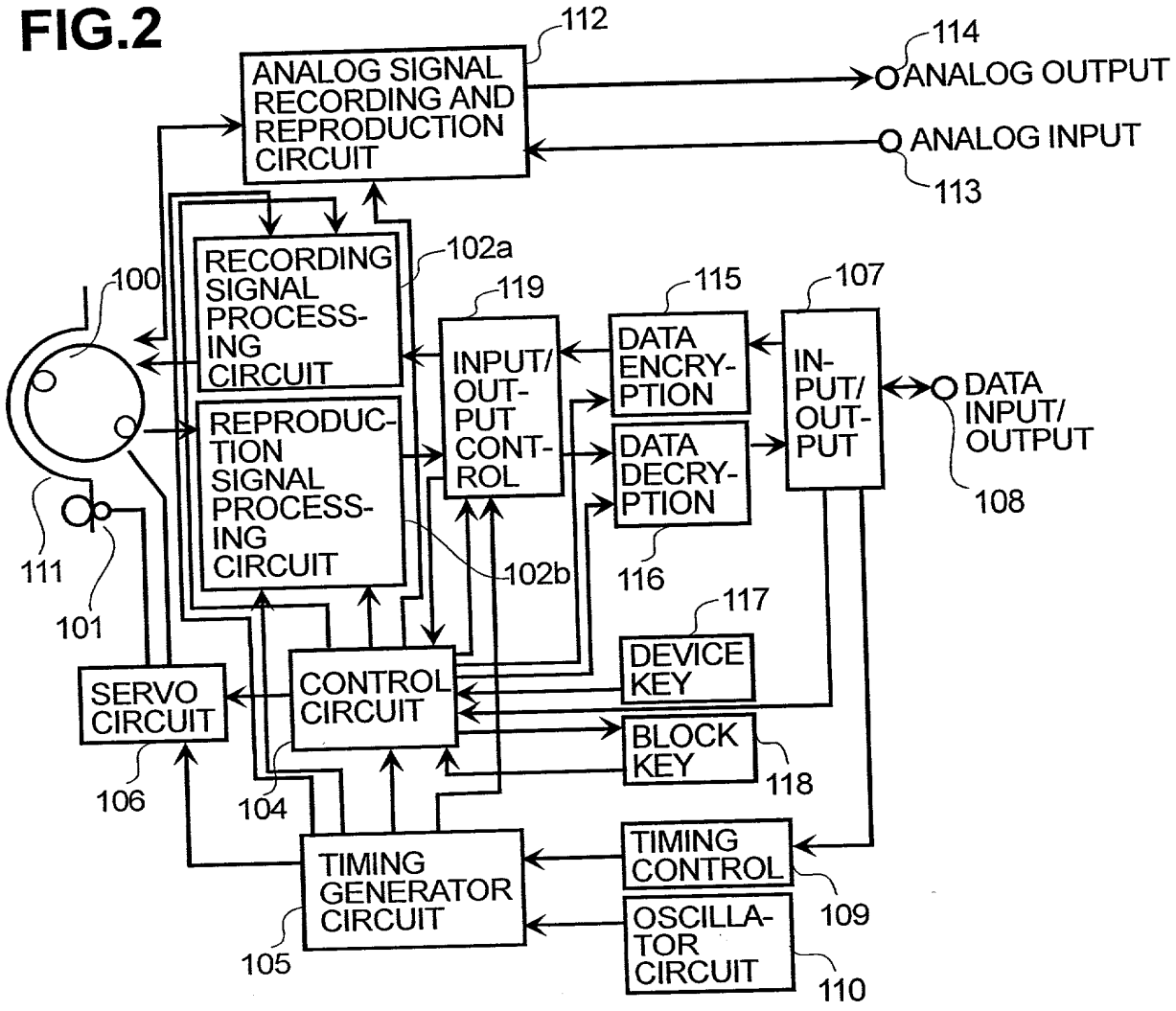

112
ANALOG SIGNAL RECORDING AND REPRODUCTION CIRCUIT
114
ANALOG OUTPUT
ANALOG INPUT
113
RECORDING SIGNAL PROCESS-ING CIRCUIT
102a
100
119
INPUT/ OUT-PUT CONT-ROL
115
DATA ENCRY-PTION
107
IN-PUT/ OUT-PUT
DATA INPUT/ OUTPUT
108
REPRODUC-TION SIGNAL PROCESS-ING CIRCUIT
102b
DATA DECRY-PTION
116
111
101
117
DEVICE KEY
SERVO CIRCUIT
CONTROL CIRCUIT
BLOCK KEY
118
106
104
TIMING CONTROL
109
TIMING GENERATOR CIRCUIT
OSCILLA-TOR CIRCUIT
105
110

FIG.3

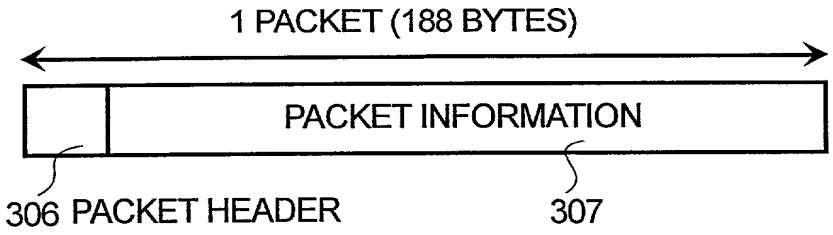


FIG.4

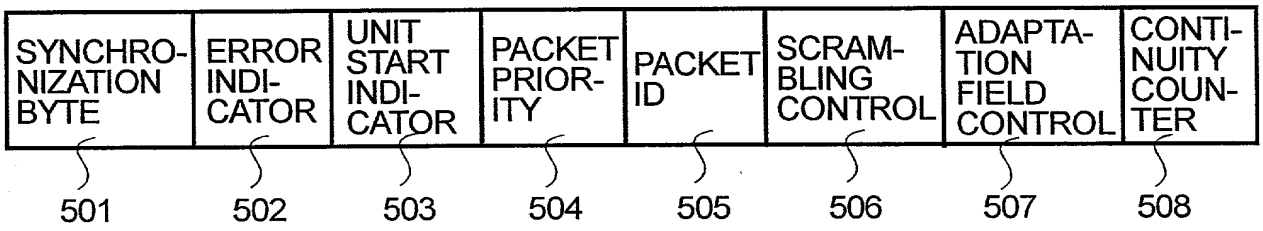


FIG.5

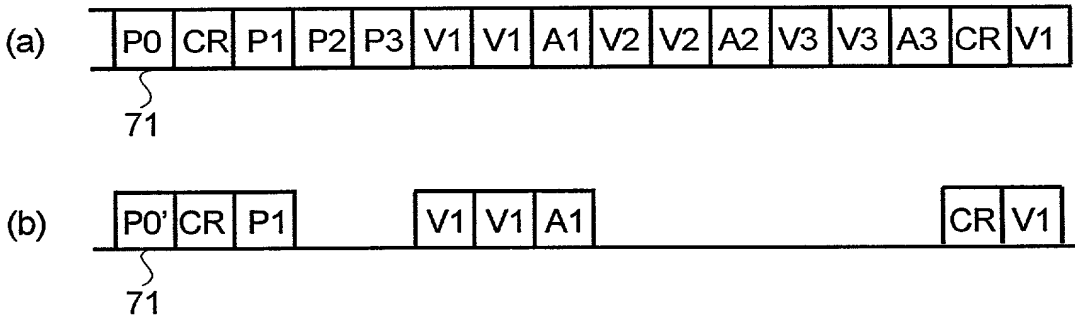


FIG.6

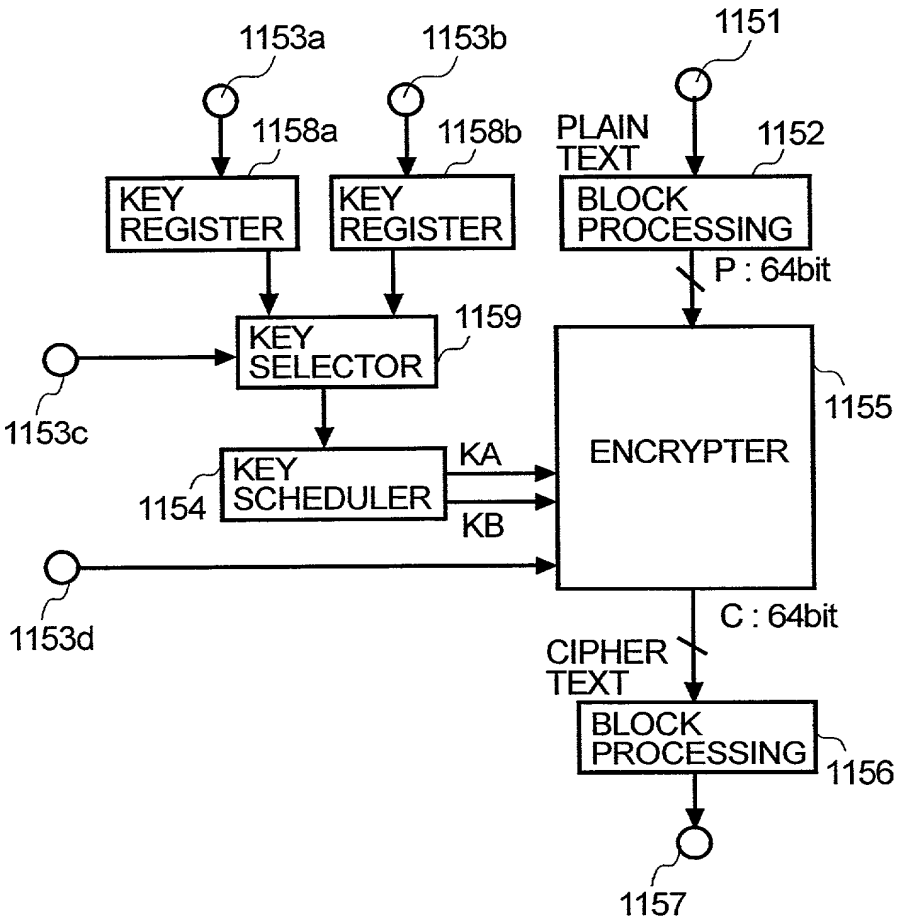

1153a
1153b
1151
1158a
1158b
PLAIN TEXT
1152
KEY REGISTER
KEY REGISTER
BLOCK PROCESSING
P : 64bit
1159
KEY SELECTOR
1153c
1155
ENCRYPTER
KA
1154
KEY SCHEDULER
KB
1153d
C : 64bit
CIPHER TEXT
BLOCK PROCESSING
1156
1157

FIG.7

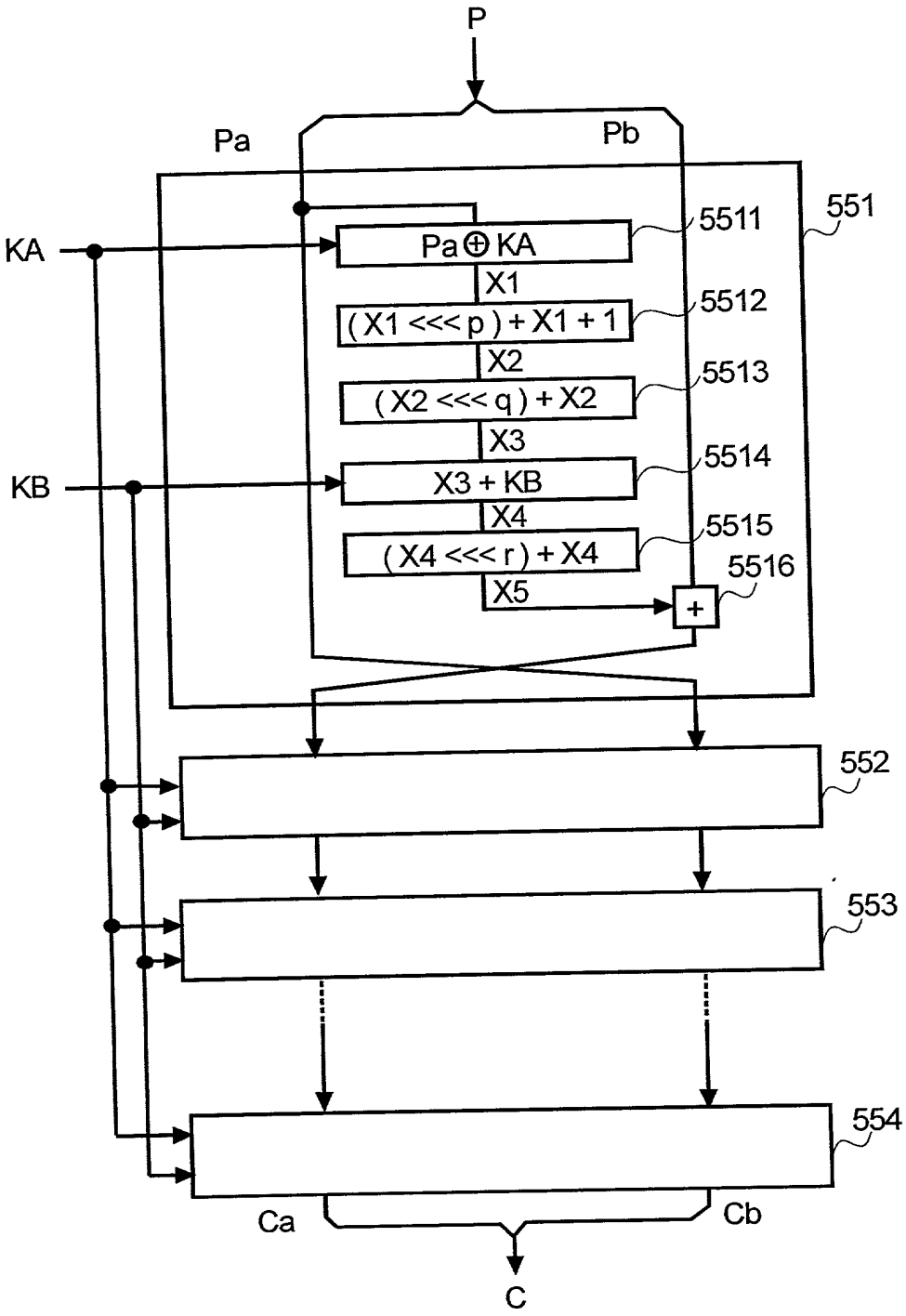

P
Pa
Pb
KA
KB
Pa⊕KA
X1
(X1 <<< p) + X1 + 1
X2
(X2 <<< q) + X2
X3
X3 + KB
X4
(X4 <<< r) + X4
X5
+
5511
5512
5513
5514
5515
5516
551
552
553
554
Ca
Cb
C

FIG.8

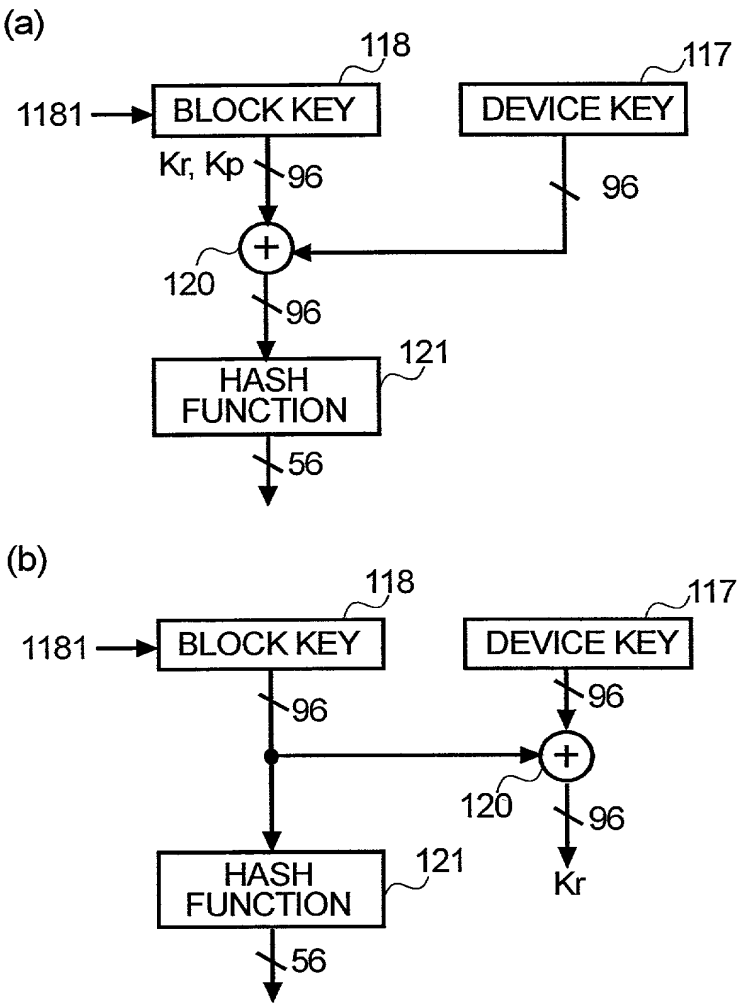

(a)
118
117
1181
BLOCK KEY
DEVICE KEY
Kr, Kp
96
96
120
96
121
HASH FUNCTION
56
(b)
118
117
1181
BLOCK KEY
DEVICE KEY
96
96
120
96
Kr
121
HASH FUNCTION
56

FIG.9

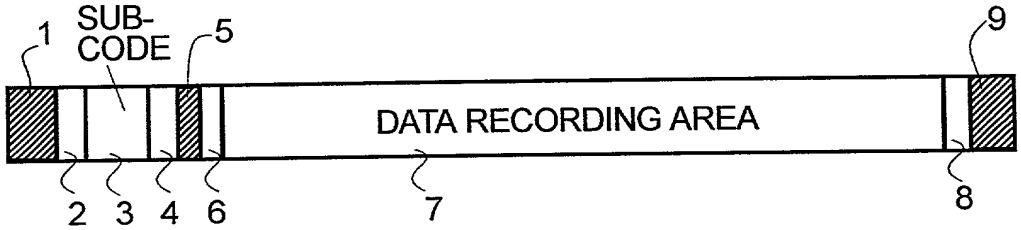


FIG.10

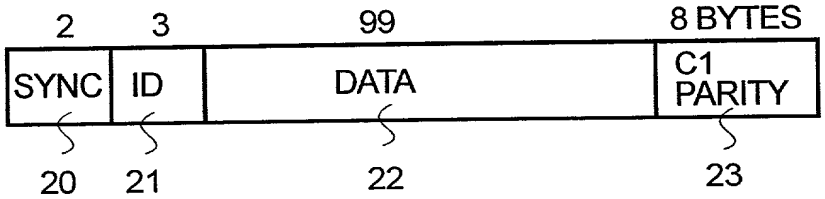


FIG.11

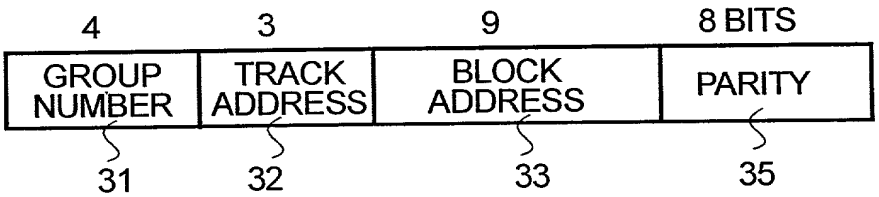


FIG.12

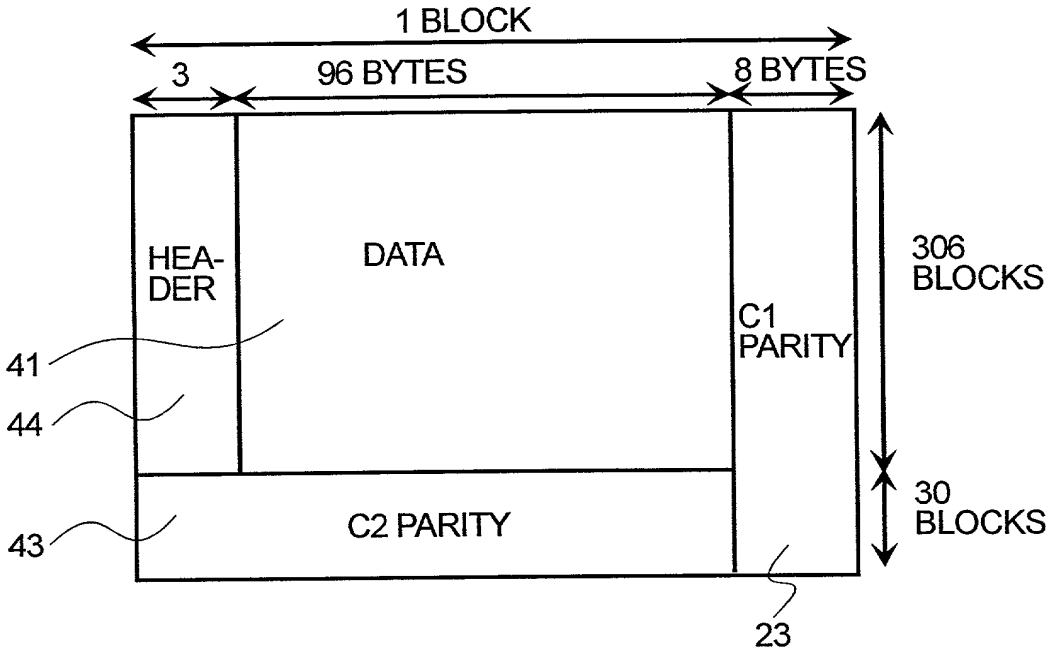

1 BLOCK
3
96 BYTES
8 BYTES
HEA-
DER
DATA
C1
PARITY
306
BLOCKS
41
44
43
C2 PARITY
30
BLOCKS
23

FIG.13

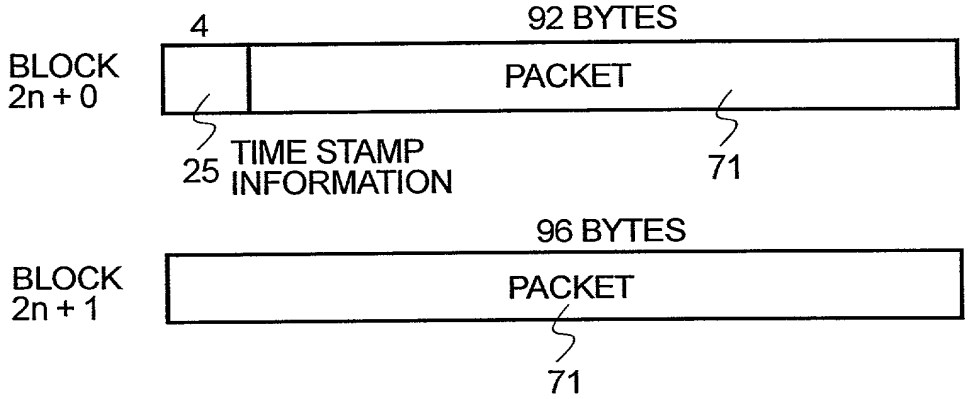

4
92 BYTES
BLOCK
2n + 0
PACKET
25
TIME STAMP
INFORMATION
71
96 BYTES
BLOCK
2n + 1
PACKET
71

FIG.14

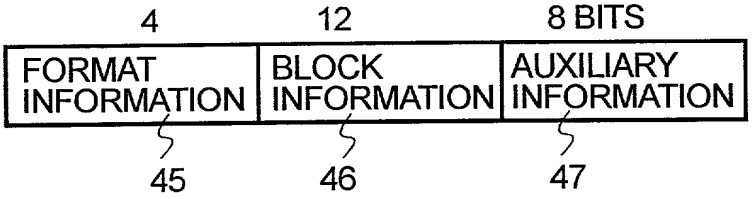

4
12
8 BITS
FORMAT INFORMATION
BLOCK INFORMATION
AUXILIARY INFORMATION
45
46
47

FIG.15

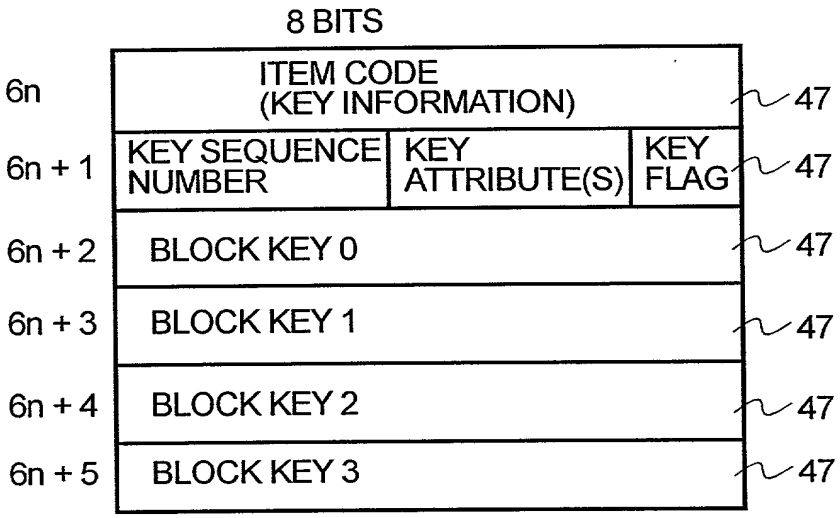

8 BITS
6n
ITEM CODE (KEY INFORMATION)
47
6n + 1
KEY SEQUENCE NUMBER
KEY ATTRIBUTE(S)
KEY FLAG
47
6n + 2
BLOCK KEY 0
47
6n + 3
BLOCK KEY 1
47
6n + 4
BLOCK KEY 2
47
6n + 5
BLOCK KEY 3
47

FIG.16

(1)

6a	" KEY INFORMATION"		
6a + 1	"2"	"0"	"0"
6a + 2	BLOCK KEY A0		
6a + 3	BLOCK KEY A1		
6a + 4	BLOCK KEY A2		
6a + 5	BLOCK KEY A3		

6b	" KEY INFORMATION"		
6b + 1	"1"	"0"	"0"
6b + 2	BLOCK KEY A4		
6b + 3	BLOCK KEY A5		
6b + 4	BLOCK KEY A6		
6b + 5	BLOCK KEY A7		

6c	" KEY INFORMATION"		
6c + 1	"0"	"0"	"0"
6c + 2	BLOCK KEY A8		
6c + 3	BLOCK KEY A9		
6c + 4	BLOCK KEY A10		
6c + 5	BLOCK KEY A11		

(2)

6d	" KEY INFORMATION"		
6d + 1	"2"	"0"	"1"
6d + 2	BLOCK KEY B0		
6d + 3	BLOCK KEY B1		
6d + 4	BLOCK KEY B2		
6d + 5	BLOCK KEY B3		

6e	" KEY INFORMATION"		
6e + 1	"1"	"0"	"1"
6e + 2	BLOCK KEY B4		
6e + 3	BLOCK KEY B5		
6e + 4	BLOCK KEY B6		
6e + 5	BLOCK KEY B7		

6f	" KEY INFORMATION"		
6f + 1	"0"	"0"	"1"
6f + 2	BLOCK KEY B8		
6f + 3	BLOCK KEY B9		
6f + 4	BLOCK KEY B10		
6f + 5	BLOCK KEY B11		

FIG.17

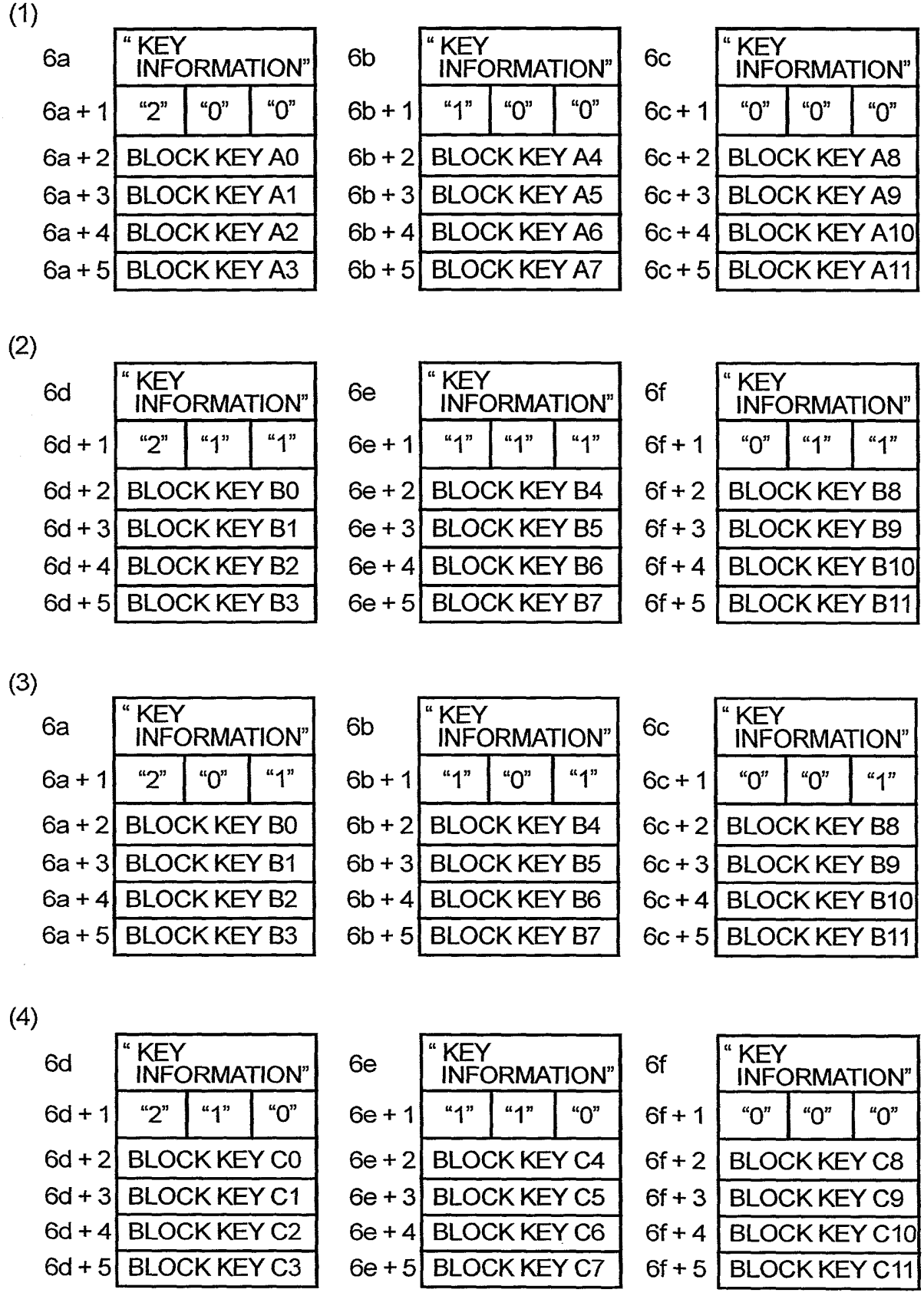

(1)
6a
" KEY INFORMATION"
6a + 1
"2" "0" "0"
6a + 2 BLOCK KEY A0
6a + 3 BLOCK KEY A1
6a + 4 BLOCK KEY A2
6a + 5 BLOCK KEY A3
6b
" KEY INFORMATION"
6b + 1
"1" "0" "0"
6b + 2 BLOCK KEY A4
6b + 3 BLOCK KEY A5
6b + 4 BLOCK KEY A6
6b + 5 BLOCK KEY A7
6c
" KEY INFORMATION"
6c + 1
"0" "0" "0"
6c + 2 BLOCK KEY A8
6c + 3 BLOCK KEY A9
6c + 4 BLOCK KEY A10
6c + 5 BLOCK KEY A11
(2)
6d
" KEY INFORMATION"
6d + 1
"2" "1" "1"
6d + 2 BLOCK KEY B0
6d + 3 BLOCK KEY B1
6d + 4 BLOCK KEY B2
6d + 5 BLOCK KEY B3
6e
" KEY INFORMATION"
6e + 1
"1" "1" "1"
6e + 2 BLOCK KEY B4
6e + 3 BLOCK KEY B5
6e + 4 BLOCK KEY B6
6e + 5 BLOCK KEY B7
6f
" KEY INFORMATION"
6f + 1
"0" "1" "1"
6f + 2 BLOCK KEY B8
6f + 3 BLOCK KEY B9
6f + 4 BLOCK KEY B10
6f + 5 BLOCK KEY B11
(3)
6a
" KEY INFORMATION"
6a + 1
"2" "0" "1"
6a + 2 BLOCK KEY B0
6a + 3 BLOCK KEY B1
6a + 4 BLOCK KEY B2
6a + 5 BLOCK KEY B3
6b
" KEY INFORMATION"
6b + 1
"1" "0" "1"
6b + 2 BLOCK KEY B4
6b + 3 BLOCK KEY B5
6b + 4 BLOCK KEY B6
6b + 5 BLOCK KEY B7
6c
" KEY INFORMATION"
6c + 1
"0" "0" "1"
6c + 2 BLOCK KEY B8
6c + 3 BLOCK KEY B9
6c + 4 BLOCK KEY B10
6c + 5 BLOCK KEY B11
(4)
6d
" KEY INFORMATION"
6d + 1
"2" "1" "0"
6d + 2 BLOCK KEY C0
6d + 3 BLOCK KEY C1
6d + 4 BLOCK KEY C2
6d + 5 BLOCK KEY C3
6e
" KEY INFORMATION"
6e + 1
"1" "1" "0"
6e + 2 BLOCK KEY C4
6e + 3 BLOCK KEY C5
6e + 4 BLOCK KEY C6
6e + 5 BLOCK KEY C7
6f
" KEY INFORMATION"
6f + 1
"0" "0" "0"
6f + 2 BLOCK KEY C8
6f + 3 BLOCK KEY C9
6f + 4 BLOCK KEY C10
6f + 5 BLOCK KEY C11

FIG.18

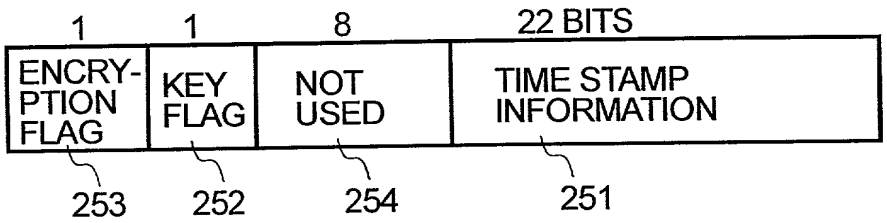

1
1
8
22 BITS
ENCRY-PTION FLAG
KEY FLAG
NOT USED
TIME STAMP INFORMATION
253
252
254
251

FIG.19

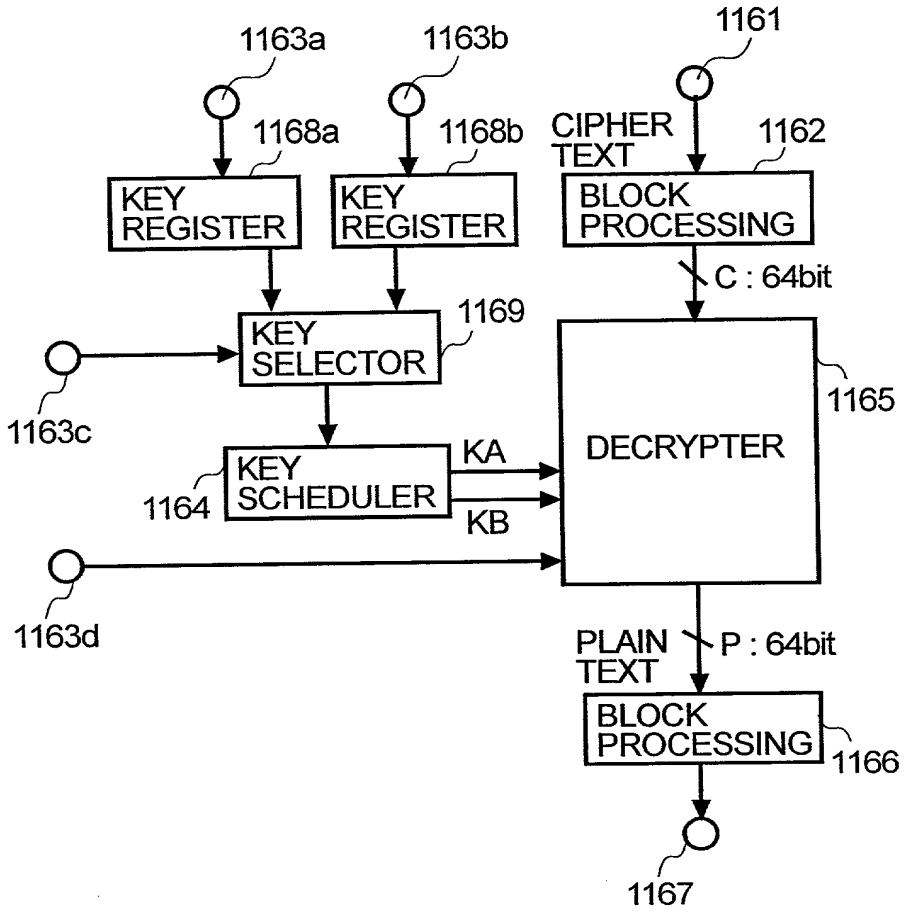

1163a
1163b
1161
1168a
1168b
CIPHER TEXT
1162
KEY REGISTER
KEY REGISTER
BLOCK PROCESSING
C : 64bit
1169
KEY SELECTOR
1163c
1165
DECRYPTER
KA
KB
1164
KEY SCHEDULER
1163d
PLAIN TEXT
P : 64bit
BLOCK PROCESSING
1166
1167

FIG.20

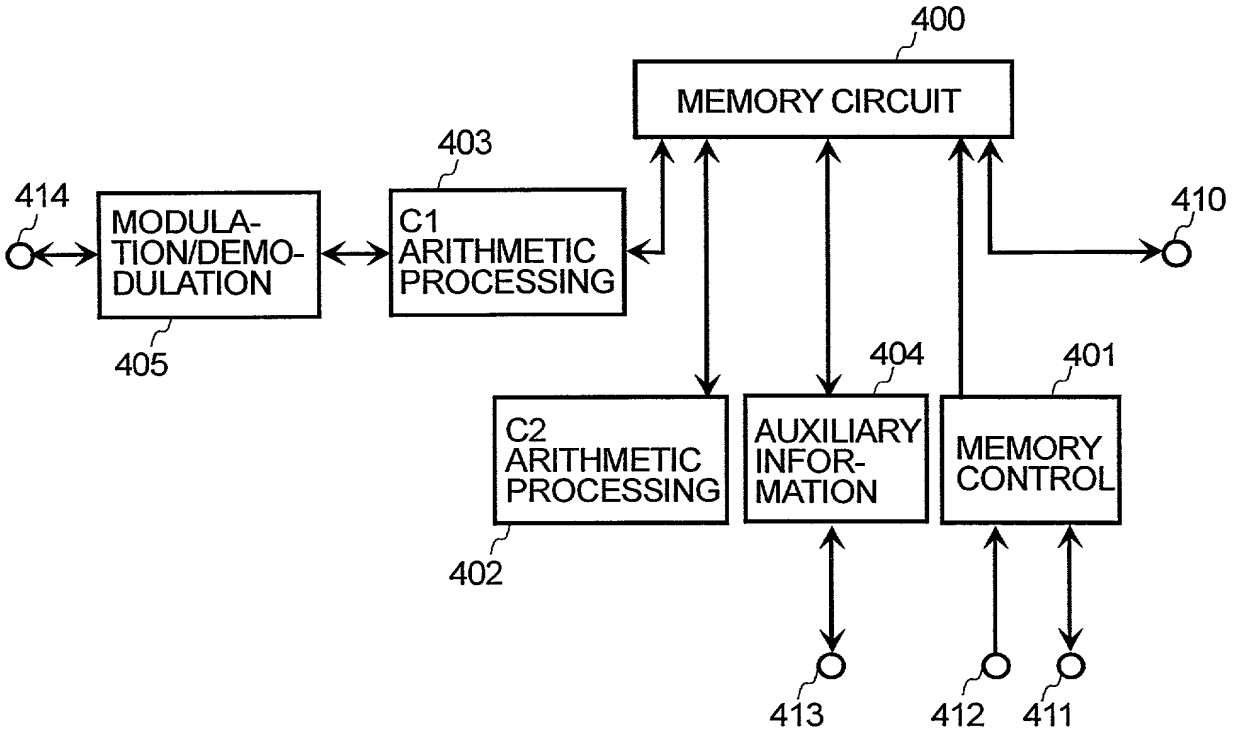

400
MEMORY CIRCUIT
403
414
MODULA-
TION/DEMO-
DULATION
C1
ARITHMETIC
PROCESSING
410
405
404
401
C2
ARITHMETIC
PROCESSING
AUXILIARY
INFOR-
MATION
MEMORY
CONTROL
402
413
412
411

FIG.21

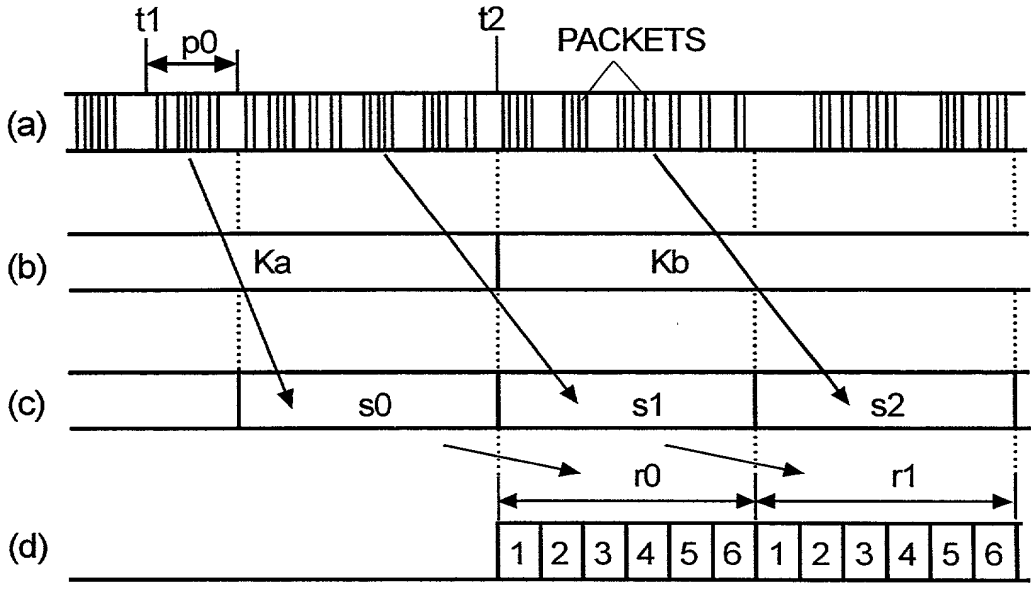

t1
p0
t2
PACKETS
(a)
(b)
Ka
Kb
(c)
s0
s1
s2
r0
r1
(d)
1 2 3 4 5 6 1 2 3 4 5 6

FIG.22

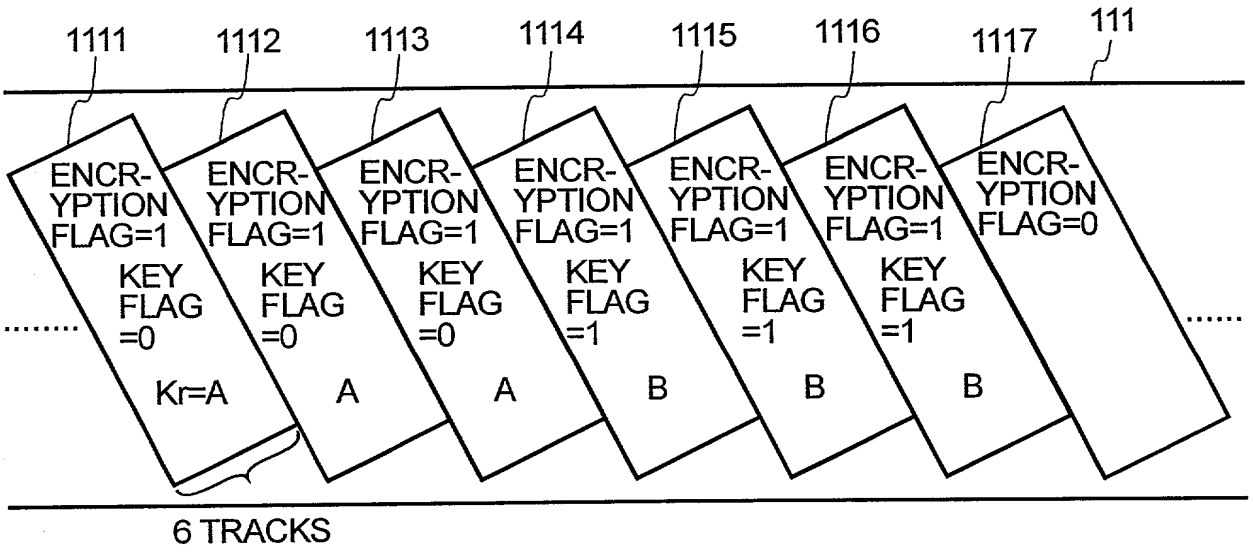

1111
1112
1113
1114
1115
1116
1117
111
ENCR-YPTION FLAG=1
KEY FLAG =0
Kr=A
ENCR-YPTION FLAG=1
KEY FLAG =0
A
ENCR-YPTION FLAG=1
KEY FLAG =0
A
ENCR-YPTION FLAG=1
KEY FLAG =1
B
ENCR-YPTION FLAG=1
KEY FLAG =1
B
ENCR-YPTION FLAG=1
KEY FLAG =1
B
ENCR-YPTION FLAG=0
6 TRACKS

FIG.23

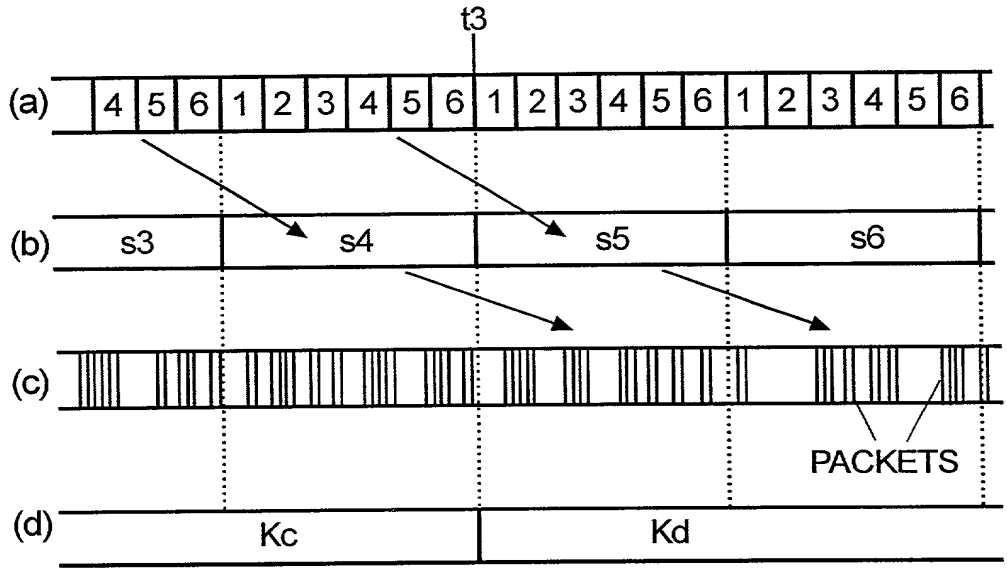
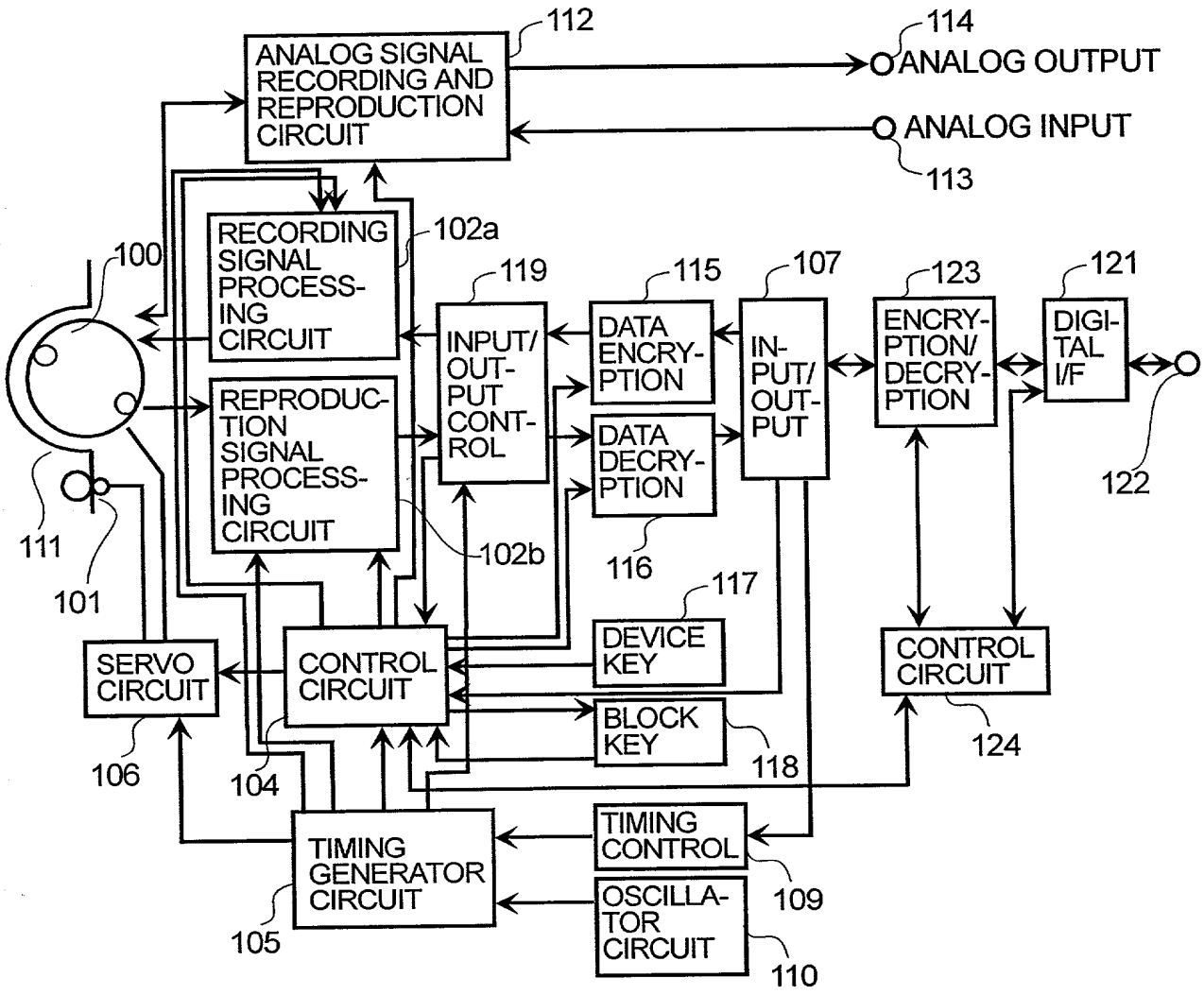

t3
(a)
4 5 6 1 2 3 4 5 6 1 2 3 4 5 6 1 2 3 4 5 6
(b)
s3
s4
s5
s6
(c)
PACKETS
(d)
Kc
Kd

FIG.24


ANALOG SIGNAL RECORDING AND REPRODUCTION CIRCUIT
112
114
ANALOG OUTPUT
ANALOG INPUT
113
RECORDING SIGNAL PROCESS-ING CIRCUIT
102a
100
119
115
107
123
121
INPUT/ OUT-PUT CONT-ROL
DATA ENCRY-PTION
IN-PUT/ OUT-PUT
ENCRY-PTION/ DECRY-PTION
DIGI-TAL I/F
REPRODUC-TION SIGNAL PROCESS-ING CIRCUIT
DATA DECRY-PTION
122
111
101
102b
116
117
DEVICE KEY
SERVO CIRCUIT
CONTROL CIRCUIT
CONTROL CIRCUIT
BLOCK KEY
106
104
118
124
TIMING CONTROL
TIMING GENERATOR CIRCUIT
OSCILLA-TOR CIRCUIT
109
105
110

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Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

DIGITAL SIGNAL RECORDER, REPRODUCER AND RECORDING MEDIUM

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
(該当する場合) _____に訂正されました。

☒ was filed on February 26, 1999
as United States Application Number or
PCT International Application Number
PCT/JP99/00929 and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

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Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）
POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

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国籍	Citizenship Japan
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(第二以降の共同発明者についても同様に記載し、署名をすること)

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第三共同発明者の署名	日付	Third inventor's signature Date Hiroo Okamoto Sep. 3, 2001
住所		Residence Yokohama, Japan JPX
国籍		Citizenship Japan
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第四共同発明者の署名	日付	Fourth inventor's signature Date Takaharu Noguchi Sept. 3, 2001
住所		Residence Yokohama, Japan JPX
国籍		Citizenship Japan
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第五共同発明者		Full name of fifth joint inventor, if any
第五共同発明者の署名	日付	Fifth inventor's signature Date
住所		Residence
国籍		Citizenship
私書箱		Post Office Address

(第六以降の共同発明者についても同様に記載し、署名をすること)

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09/913595

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